IS THE SEARCH FOR RAD-HARD CHIPS ON TRACK?/82

THE PROMISES AND PITFALLS OF HIRING TEMPORARY HELP/91

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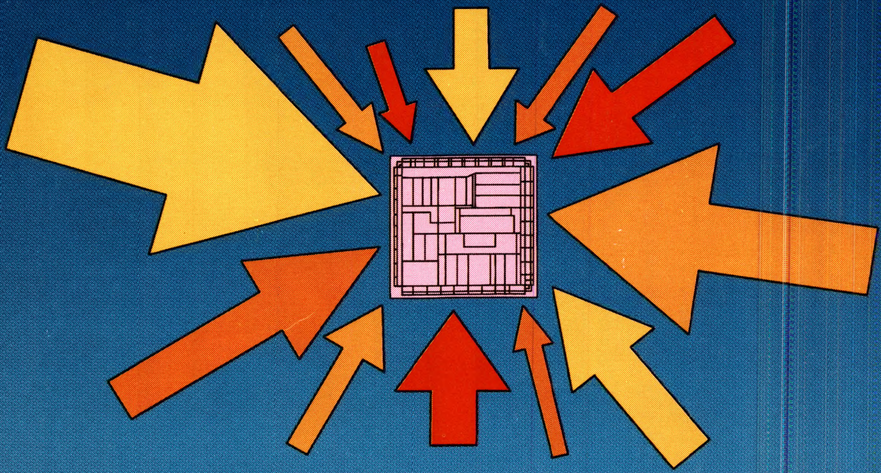

MICROPROCESSORS

PAGE 70

RISC, CISC, AND CRISP—THEY ALL MEAN MORE POWER, MORE SPEED, AND MORE FEATURES, BUT HOW DO YOU CHOOSE?

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TERADYNE

Circle 19

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SO YOU'VE GOT A MILLION TRANSISTORS

As a new communications art form, today's mega-microprocessor announcements are a tough act—of faith—to follow

We are about a month shy of announcing a full line of components based on deuterium-enriched palladium. However, even if we had that story in the bag, it would still probably have yielded up this issue's cover to the microprocessor report (p. 70). No matter how you cut it—RISC vs. CISC, Intel against Motorola, quantum leaps for hardware opposed to the Black Hole of lagging software development—the microprocessor circus is today's hot ticket.

There was a time when you could say with certainty that, as an industry-wide syndrome, the marketeers were constantly co-opting the techies. Now, very possibly, things have swung the other way. Processor performance has outstripped even the ad writers' capacity for the appropriate hyperbole. For example, the frustrated wordsmith charged with polishing one trade ad for Sun's new SPARCstation could but refer to its "blinding speeds"—which is certainly an attribute I would prefer not to see (pardon the pun) in *my* work station. At the same time, responsible, technically grounded managers like Intel's microprocessor chief, David House, can look you right in the eye and promise, because his company's new 80486 is such a wonderfully compatible chip off the old block, to "protect your $15 billion software investment."

I don't know of any discrete organization—even one that might have paid full price—with anything like $15 billion tied up in software. House can be excused, of course, because he was—or believed he was—addressing an entire universe.

It is not wrong to think in terms of marketing to a universe. It could be a trap, however, to forget that universes are composed of individual users. Individual users who, over the course of the ensuing year, will have an opportunity to discover for themselves that mips can be manipulated, flops will fluctuate, that pipelines can stall, and that a superfast CPU coupled with available commodity RAM can amount to a floating submarine. Thus, from that perspective, does the power and glory of the typical new microprocessor run downhill, these days, from the time of its introduction. The higher its raw, naked power at birth the more it may seem, in eventual system configuration, to degrade.

All of which is to say that, ultimately, the delivery of total systems performance—real-world value—is what will determine the true merit of these wonder chips. It may be worth pausing to consider something that used to be called the home-computer market. According to the San Francisco consulting firm Volpe & Covington, American households are currently throwing out computers at the rate of 1.3 million per year, or about one for every three that are being installed. These are mostly toylike machines, many that cost less than $500, bearing little resemblance to the PCs people buy for home use today. But inside some of them you'll find microprocessors that were called, in their day, miraculous.

ROBIN NELSON

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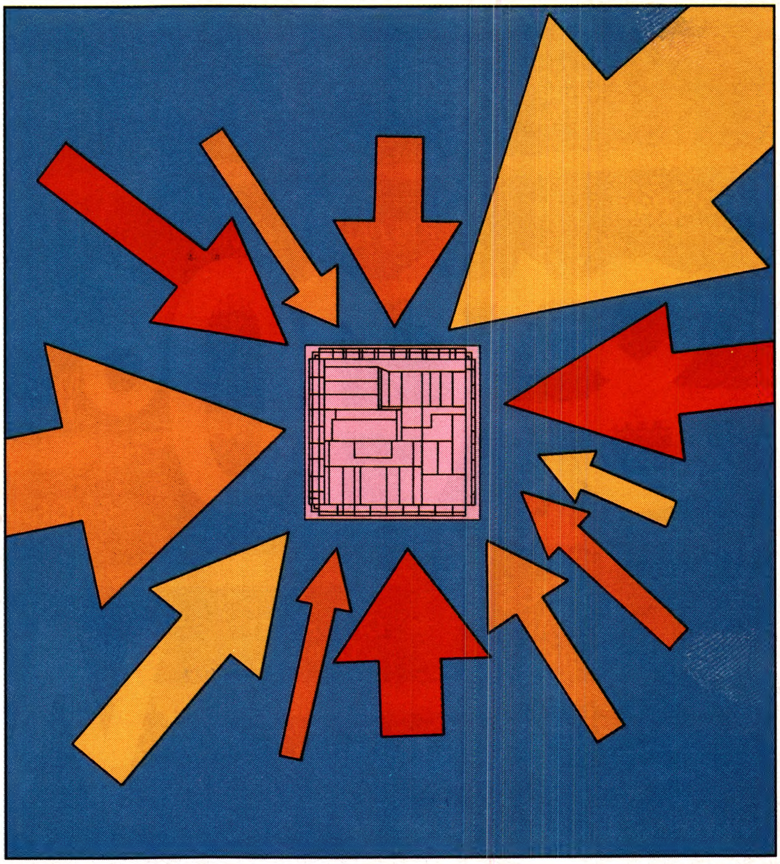

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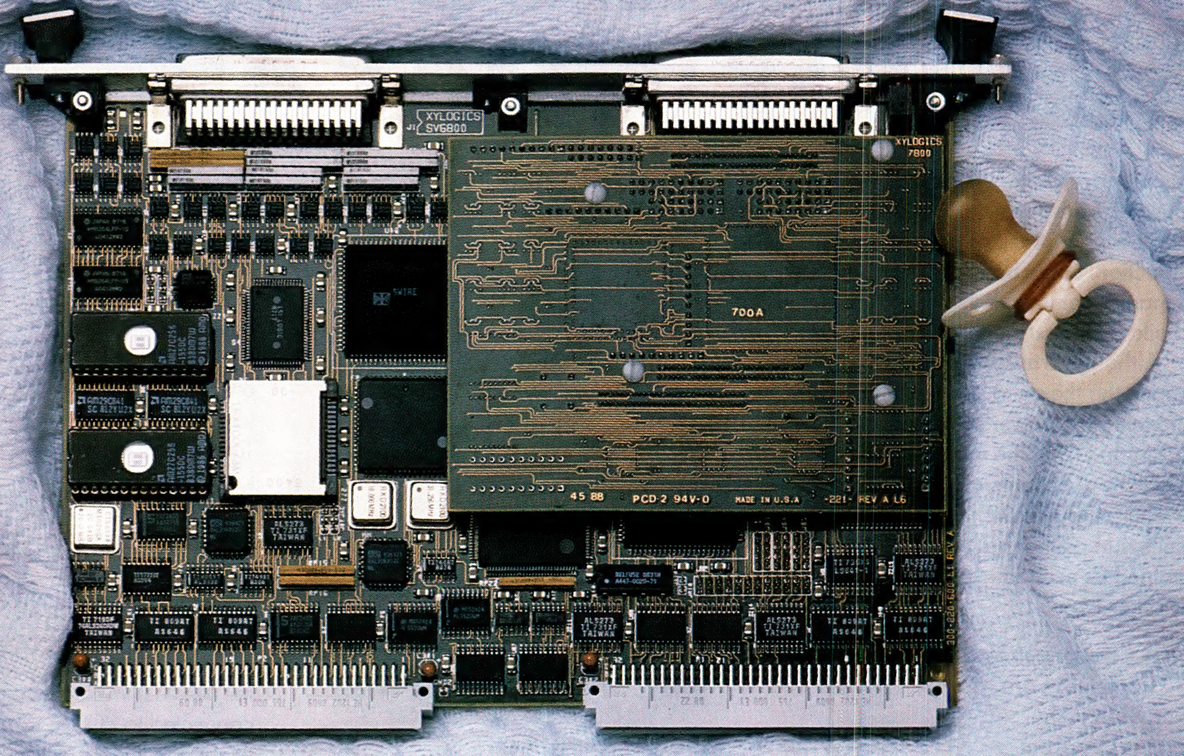

Born yesterday, and already talking 20 megabytes a second.

The new SV Series IPI-2 VME disk controllers from Xylogics. . .a prodigy of data rate performance.

Xylogics announces the SV7800 and SV6800 single-board disk controllers for VMEbus systems that will more than triple the disk data transfer rate currently available. With internal data paths up to 80 MB/sec, the SV Series controllers can sustain a data rate across the VMEbus of more than 35 MB/sec. This more than doubles the rates of current controller solutions. And our SV Series features a new ''Universal Bus Silicon'' architecture that sets the stage for future generations of controllers.

Addressing a critical market need for faster, higher capacity disk storage at an affordable price, the SV7800 and SV6800 IPI-2 controllers are the new standard for data-intensive applications such as supercomputing, real-time data acquisition, graphics, imaging and electronic publishing. And RISC users will find the SV Series eliminates major disk I/O bottlenecks.

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Circle 18

PUTER'S TERRIFIC, AL APPLICATIONS?”

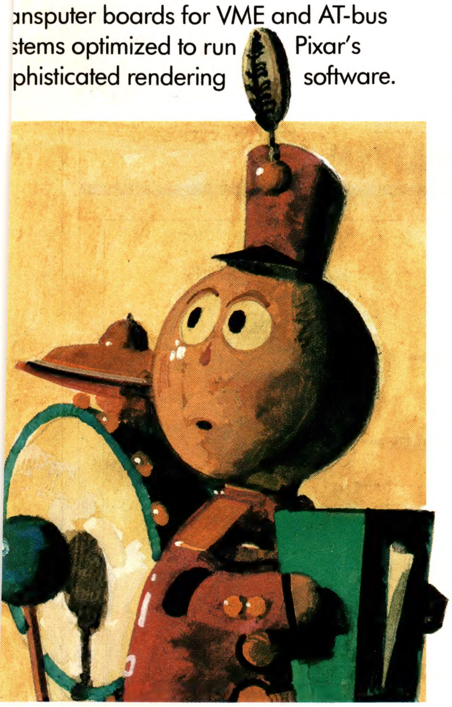
ght Simulation

British Aerospace have used
nsputers to develop a low-cost
nt simulator comprising a flat
rld, ground-
d, buildings,
es and mountains –
n an optional Head-
display. Future enhancements
include the addition of undulating
rain and a single or triple window
play option.

American companies are also using
nsputers to build high-performance
ht simulators more cheaply. One U.S.
nufacturer utilizes over one thousand
00 processors per system.

D Rendering

Pixar in the US has developed a
nspuuter-based rendering system which
ickly renders photorealistic images from
D models. The system consists of
nsputer boards for VME and AT-bus
stems optimized to run Pixar's
phisticated rendering software.



The system holds great promise for such
pplications as architecture, automobile
yling, package design, simulation as well
s animation. Pixar's recent computer
enerated film 'Tin Toy' could not have
een done without using this
ransputer-based accelerator.

System Control

As the number of Transputers in a system design are increased, a proportional increase in performance can be achieved.

In West Germany, Parsytec GmbH is using this principle in their Megaframe Superclusters. Superclusters represent a complete series of reconfigurable industrial control boards as used in the automotive industry, which exploit the Transputer's parallel processing capability.

The basic Model 64, built with T800's, has a performance of 640 MIPS and 96 MFLOPS. The Model 256 comprises four Model 64 cabinets connected by cables and provides 2,560 MIPS and 384 MFLOPS.

Parsytec believes there is no limit to the size Superclusters can grow to. Two Model 256s can be combined easily to realize twice the raw performance of one system.

Robotics

Transputers are ideally suited for robotics applications because their special on-chip links make communication between control centers naturally easy. They are often used in the central control area for dumb robots, in multi-jointed robots, and in machine vision systems.

At the Houston Space Center, NASA and Lockheed are using Transputers in the development of an intelligent, self-manoeuvering, voice-controlled robot named EVA Retriever. EVAR is being built to investigate the autonomous retrieval of objects and astronauts that become detached from the Space Station.

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Throughout the AB Group the total reliability concept is achieved through a manufacturing policy of 'zero defects'. High quality AB components and systems are found in data processing, telecoms, automotive and consumer products, as well as in a wide range of aerospace and defence equipment.

The AB Group has nineteen operating companies world-wide and provides a total capability in the design, development and manufacture of electronic and electro-mechanical components and sub-systems. Investment in CAD/CAM/CAE, a Group technology centre, and extensive surface mounting facilities has taken AB to the forefront of electronic design and production technology.

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Circle 7

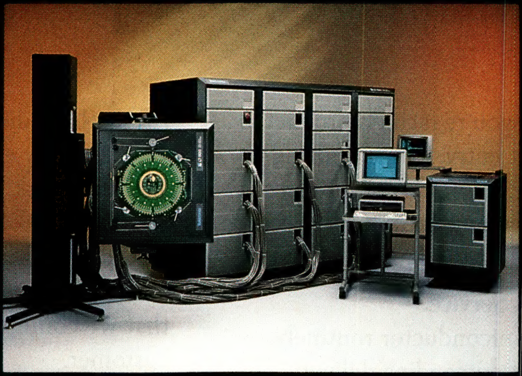
"$4.5 million to test a 500-pin chip we don't even make yet?"

No. Because now there's the Vista Series from Tektronix. A 512-pin ATE solution for less than $1.5 million. Ready for today's IC testing challenges — and tomorrow's.

Unprecedented flexibility.

The Vista Series VLSI Logic Test Systems feature an innovative modular architecture for unprecedented system- and site-level flexibility.

Systems are configured with three modules: the Test Station, the Program Development Station, and the Auto-Calibration Station. Systems can be configured for initial functionality and capacity requirements, and then economically expanded on-site to meet new demands. The result is a lower initial system cost combined with an economical future growth path.



Teknology pays off.

At Tektronix, we don't have to go shopping for innovative technology. We make our own. It's called Teknology. Teknology is employed throughout the Vista Series architecture. For example, we designed custom high-speed CMOS ASICs for the pin electronics. Replacing conventional hybrid circuits with advanced IC technology increased system performance and uptime. At the same time, total cost for a 512-pin system was lowered to less than $1.5 million from usual ranges of $3 to $5 million. And since these proprietary CMOS ASICs consume less power and emit less heat than their hybrid counterparts in our competitors' systems, operating costs are reduced more than 80 percent.

Tektronix — committed to the future.

Tektronix has been delivering state-of-the-art electronics for more than 40 years. Setting the standard by which test instrumentation is judged.

The Vista Series. Economical, state-of-the-art ATE. Another standard. Proof that you don't have to spend $4.5 million for an ATE solution — today *or* tomorrow.

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Circle 38

ELECTRONICS NEWSLETTER

MOTOROLA JUMPS INTO THE IBM PC-CLONE ARENA . . .

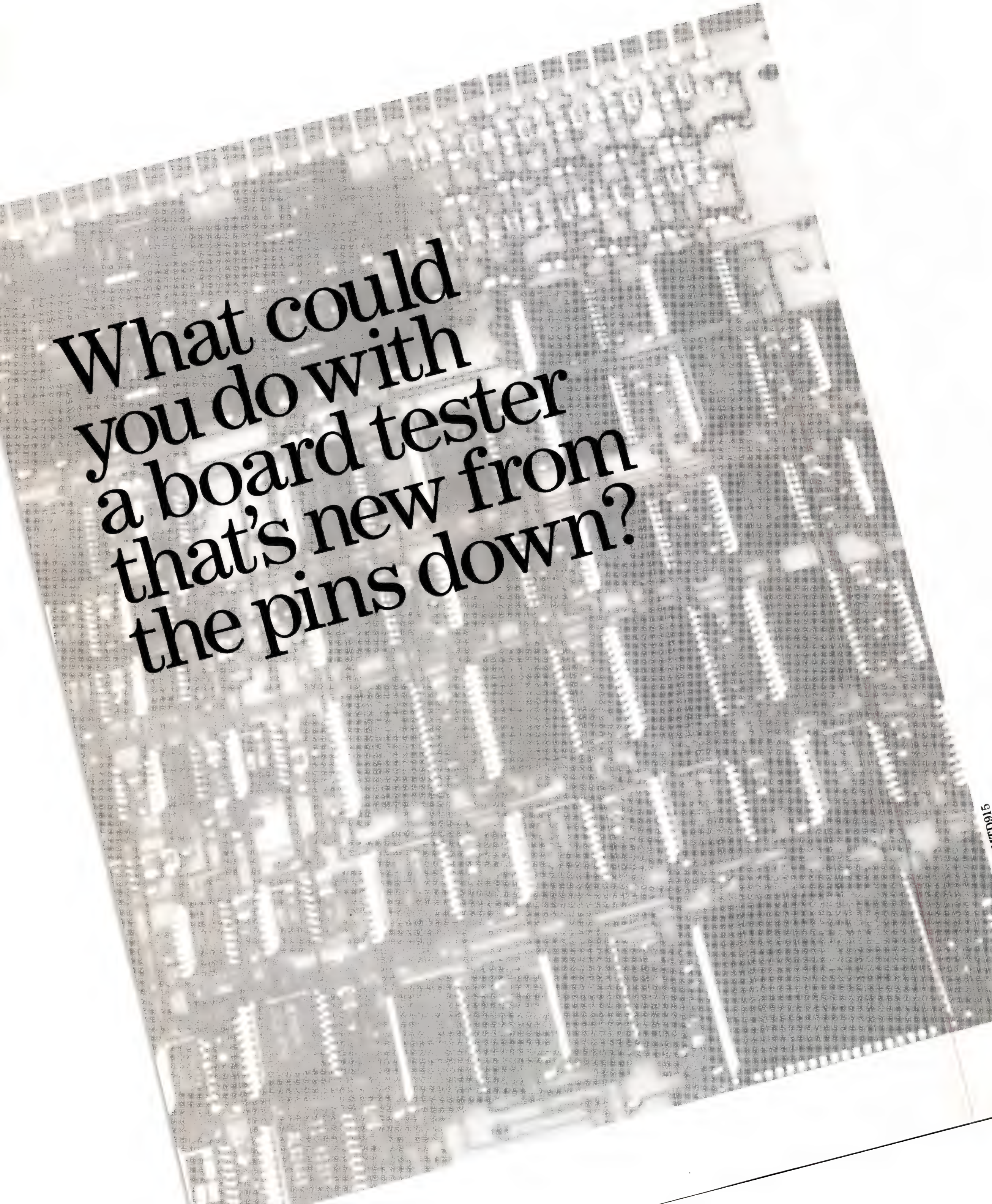
It seems pretty strange on the face of it that Motorola Inc. would make products to support the microprocessors of archrival Intel Corp. But the new products are microcomputer chip sets for making IBM Corp. Personal Computer AT clones, which are built around Intel processors. Motorola will market two chip sets for PC AT-compatible machines: one that supports the Intel 80286 and one for the higher-powered 80386 processor. The chips come to Motorola by way of an alliance with ACC Microelectronics Corp. of Taiwan. Motorola's Semiconductor Products Sector in Austin, Texas, has acquired from ACC the rights to manufacture and sell that company's ACC82020 chip set for 16- and 20-MHz PC AT-compatible computers and the ACC82300 set for the 20-to-25-MHz 386 machines, as well as the ACC16C451 family of multifunction input/output controllers. ☐

. . . AND VIA TECHNOLOGIES LOOKS TO CHALLENGE THE LEADERS

As Motorola gears up to enter the IBM Personal Computer-clone chip-set market, one of the sector's established players—Via Technologies Inc. of Fremont, Calif.—is pitting its next generation of chips against those of market leaders Chips & Technologies, G2, and Intel/Zymos. Via's modular SL90XX Generic PC AT Core Logic Set attacks one problem plaguing PC-clone chip sets: partitioning. "Functions that require critical timing and speed, such as high-speed memory control, have typically been spread over the multiple chips in the set," says Idris Kothari, vice president of engineering. Making all these chips fast enough can destroy any price advantage the chip set would have over a discrete solution, he says. Via is putting all the critical timing functions on one high-performance universal-clock chip. A core logic set that doesn't require critical timing is also offered; it can be used in all Intel 80286- and 386SX-based computers, as well as in 386 systems using the AT bus. The Via chip set includes four controller chips—one each for the system, data, addresses, and peripherals—and memory-controller chips that can be tailored to a specific system-design architecture. The result, claims Via, is a chip set with optimum partitioning that offers the right performance for each PC system, at a cost below that of discrete parts. ☐

CONTROL DATA BOWS OUT OF THE SUPERCOMPUTER BUSINESS

The supercomputer business is getting so competitive that even the pioneer of supercomputing can't keep up the pace. Control Data Corp., which as the inventor of supercomputers has been in the business longer than any other company, announced last month that it was discontinuing its ETA Systems supercomputer division. The Minneapolis-based computer maker had spun off ETA Systems as a separate company about five years ago to build the follow-on to Control Data's Cyber 205 supercomputer. At the time, Control Data hoped to get additional financing for ETA by selling part of the operation to other investors. Although outside money didn't exactly flow freely, Control Data kept ETA Systems going by funding the ETA-10 development project, with the aim of building the world's most powerful supercomputer, itself. The spin-off company successfully developed a broad family of very powerful parallel supercomputers using high-density CMOS technology, a development effort that culminated in the mighty ETA-10 machine. But sales lagged, and last October Control Data brought ETA Systems back into the fold as a division in an attempt to stem the losses. Competition from Cray Research Inc. and Convex Computer Corp. in the U. S. and looming competition from the biggest Japanese computer companies inflicted severe losses on ETA Systems. Control Data won't say what it spent on ETA, but the company acknowledges losing $100 million in the supercomputer business last year. ☐



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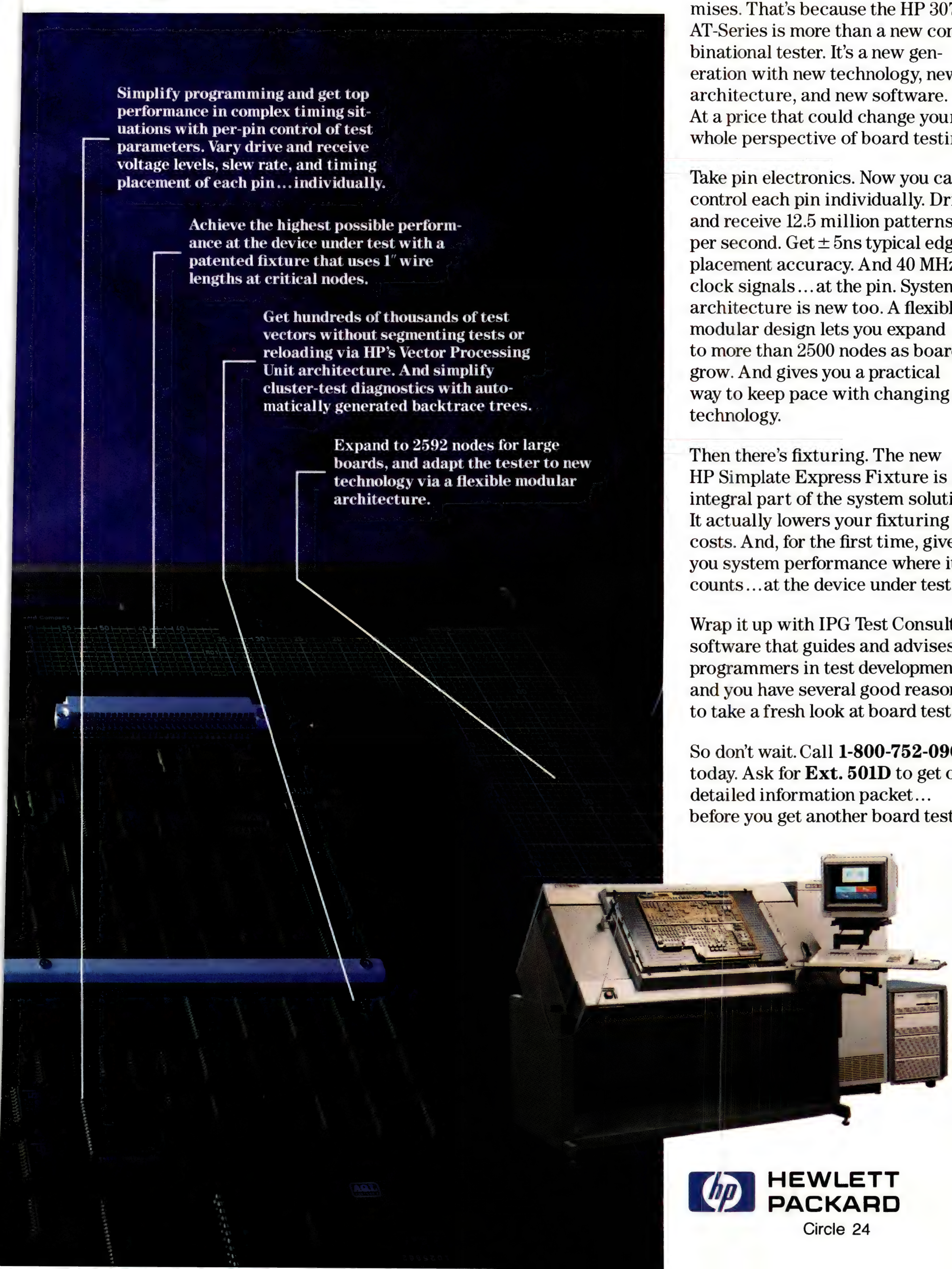
testing of complex boards…



Simplify programming and get top performance in complex timing situations with per-pin control of test parameters. Vary drive and receive voltage levels, slew rate, and timing placement of each pin…individually.

Achieve the highest possible performance at the device under test with a patented fixture that uses 1″ wire lengths at critical nodes.

Get hundreds of thousands of test vectors without segmenting tests or reloading via HP's Vector Processing Unit architecture. And simplify cluster-test diagnostics with automatically generated backtrace trees.

Expand to 2592 nodes for large boards, and adapt the tester to new technology via a flexible modular architecture.

Here's the advanced tester you've been looking for. With no compromises. That's because the HP 3070 AT-Series is more than a new combinational tester. It's a new generation with new technology, new architecture, and new software. At a price that could change your whole perspective of board testing.

Take pin electronics. Now you can control each pin individually. Drive and receive 12.5 million patterns per second. Get ± 5ns typical edge placement accuracy. And 40 MHz clock signals…at the pin. System architecture is new too. A flexible modular design lets you expand to more than 2500 nodes as boards grow. And gives you a practical way to keep pace with changing technology.

Then there's fixturing. The new HP Simplate Express Fixture is an integral part of the system solution. It actually lowers your fixturing costs. And, for the first time, gives you system performance where it counts…at the device under test.

Wrap it up with IPG Test Consultant software that guides and advises programmers in test development and you have several good reasons to take a fresh look at board testing.

So don't wait. Call **1-800-752-0900** today. Ask for **Ext. 501D** to get our detailed information packet… before you get another board tester.

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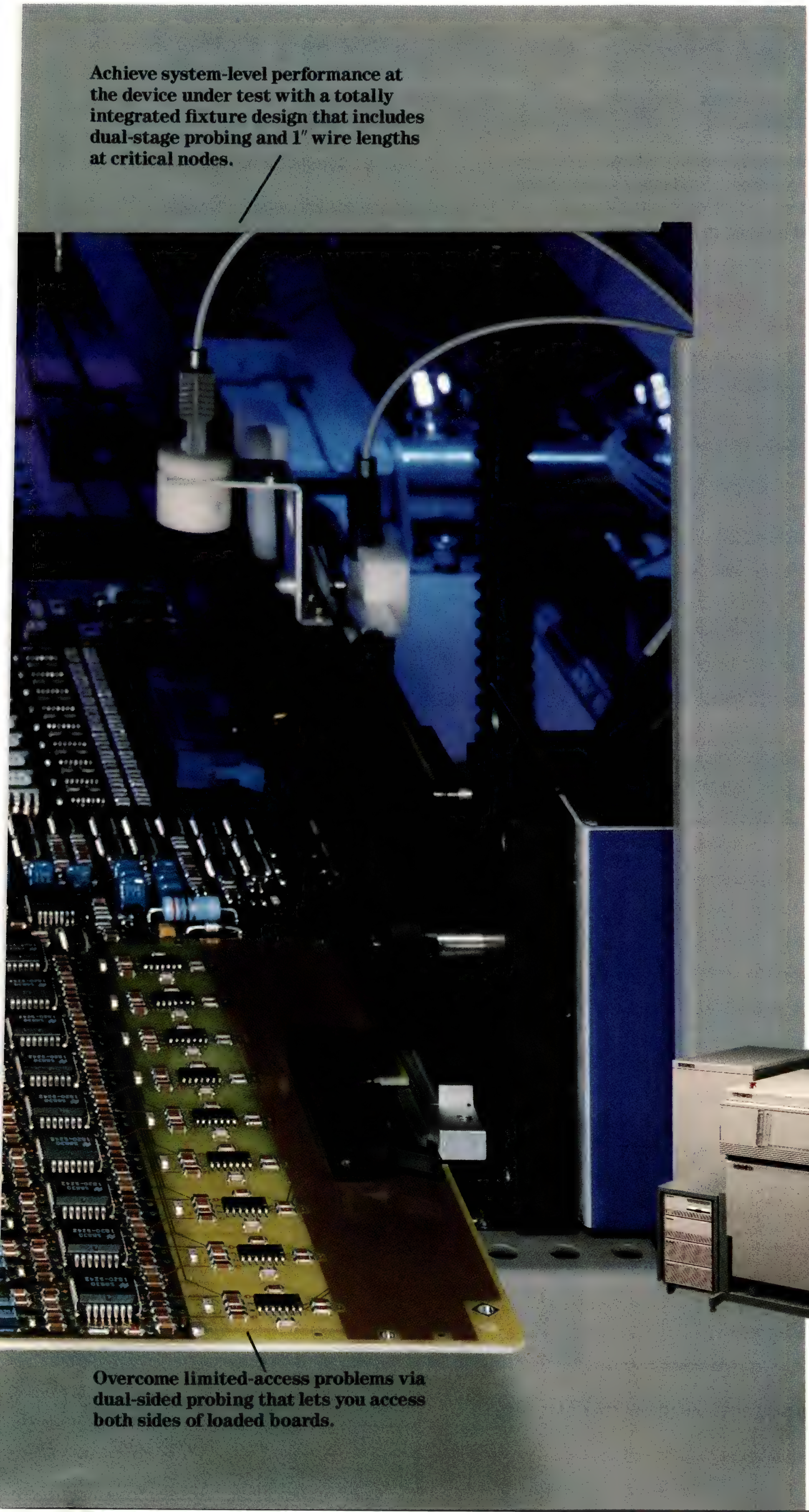
Circle 24

SMT board testing problem.


Achieve system-level performance at the device under test with a totally integrated fixture design that includes dual-stage probing and 1″ wire lengths at critical nodes.
Overcome limited-access problems via dual-sided probing that lets you access both sides of loaded boards.

Here's a real board-test breakthrough. The new HP 3070 SMT-Series combinational tester will challenge your belief that SMT boards are hard to test. We've solved the problems. Which gives you the go-ahead on SMT production. Here's how.

First, an innovative mechanical fixturing system handles high-accuracy, dual-level, dual-sided probing. Without flexing boards, which can mask open solder joints or create new process faults. You can even integrate it easily into automated SMT lines.

Then, a new system architecture and pin electronics deliver the tester performance you need for SMT devices such as ASICs. For example, you can control each pin individually. Drive and receive 12.5 million patterns per second. Get ± 5ns typical edge placement accuracy. And 40 MHz clock signals...at the pin.

You also get a surface-mount-device library to decrease test development time for nonstandard pin-out devices. Plus IPG Test Consultant software, which acts as an advisor in test development and simplifies quality management.

So if board testing has been a roadblock to SMT integration, investigate the HP 3070 SMT-Series. It's sure to give you a new perspective. Call **1-800-752-0900** today. Ask for **Ext. 501E** to get our detail packed information package on SMT board testing.

HEWLETT PACKARD
Circle 25

PRODUCTS TO WATCH

WHILE SILICON COMPILER SYSTEMS ATTACKS THE TURNKEY DESIGN MARKET . . .

Breaking out of its high-end niche of tools for custom integrated-circuit design, Silicon Compiler Systems Corp. is introducing a modular product family that integrates its leading-edge software with existing circuit-design environments. The San Jose, Calif., company's new Explorer Series comes in three versions: SCS Foundation lets highly specific design tools developed in-house by customers work with Silicon Compilers' software suite; Explorer Tools are 15 modular programs for design entry, synthesis, simulation and analysis, and physical design and test; and Explorer Design Systems are six preconfigured IC design schemes optimized for custom and application-specific chips. The systems address the needs of a broad range of designers, from logic designers using ASICs to layout engineers in standard-part design groups. Explorer Series products are available now and run on Unix-based hardware from Apollo Computer, Digital Equipment, and Sun Microsystems. □

. . . SIERRA SEMICONDUCTOR MELDS DIGITAL AND ANALOG DESIGN TOOLS

Sierra Semiconductor Corp. has overcome the speed problems that plagued previous attempts to combine digital and analog design tools. While other design packages use separate analog and digital simulators, the San Jose, Calif., company has integrated its proprietary mixed-signal simulator algorithms into Silicon Compiler Systems Corp.'s schematic-capture software and Lsim logic simulator. The resulting software—called Montage—takes 11 seconds to simulate designs that a Spice simulator does in 6 hours. It includes simulation models from Sierra's 300-cell library, including 25 analog circuits, more than 245 digital parts, and nine electrically erasable read-only memories. Priced at $29,500, Montage now runs on Sun Microsystems Inc. work stations and will run on Apollo Computer Inc. machines later this year, the company says. □

CREE ADDS LOW-COST BLUE TO THE LIGHT-EMITTING DIODE SPECTRUM

A tiny Durham, N. C., company has developed a silicon-carbide blue-light-emitting diode that will sell for a small fraction of the $45 to $80 charged by giants like West Germany's Siemens AG and Japan's Sanyo Electric Co. for similar LEDs. Cree Research Inc. is pricing volume quantities at $2 apiece packaged and $1 unpackaged. Samples are priced at $40. Used with readily available red and green LEDs, the low-cost blues mean LED displays can now compete with incandescent lights in giant-screen displays for stadiums and other applications. The new diodes can also be used in digital color printers and medical equipment, where there is a need for near-ultraviolet light sources. Cree plans to offer a variety of diodes, ranging from single-color LEDs to chips that will emit multiple wavelengths and colors. □

SIGNETICS CHIP SET SHRINKS CELLULAR-PHONE CHIP COUNT BY 60%

The next generation of pocket-size, battery-powered cellular-radio handsets gets a boost from a six-chip set from Signetics Corp. Four CMOS and two bipolar circuits cut chip count in cellular phones by up to 60%, says the Sunnyvale, Calif., company. Other mobile-radio applications will benefit as well. The CMOS chips include the UMA1000, which handles filtering associated with cellular-control data, supervision, and signaling; the 80C552 microcontroller; the NE5751 audio-band filter; and the TDD1742 frequency synthesizer. The two bipolar parts are the NE5750, which integrates compaction/expansion, noise canceling, power amplification, and control functions, and the NE605 FM IF mixer/oscillator, amplifier, and demodulator. Available in September, the chip set will cost less than $60 in high-volume purchases. □

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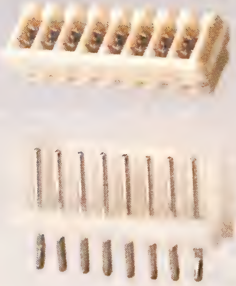

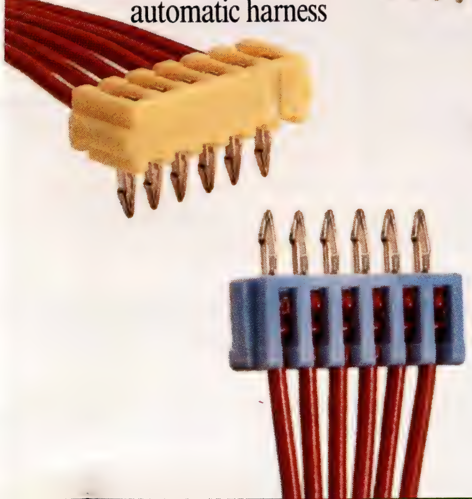

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Electronics

MOTOROLA TAKES THE WRAPS OFF COMMODITY-MEMORY THRUST

Word is out—the semiconductor giant is producing DRAMs and SRAMs in volume

AUSTIN, TEXAS

In an industry where secrets can seldom be kept for long, Motorola Inc.'s success in keeping its commodity memories program under wraps is exceptional. Despite the attention generated by an all-out, three-year effort that reportedly has cost some $300 million, executives in the company's Semiconductor Sector and MOS Memory Products Division have been able to keep details from leaking. Until now, Motorola has shared information about the project, one of the most ambitious currently being attempted by a major U. S. chip maker, only with major customers.

This period of self-enforced silence is coming to an end, however. Motorola's effort, with the aid of a pact with Toshiba Corp., to build its presence in the memory market has now passed a critical point. In recent months, the company has taken some giant strides in establishing a solid base in the memory market—and now it's talking about them.

MOTOROLA'S MEMORY ROADMAP

Technology (in microns)	Products		Development start	Introduction date	Peak output
	SRAM	DRAM			
1.8	64 Kbit	256 Kbit	1977	1982-83	1988
1.2	256 Kbit	1 Mbit	1980	1985-86	1991
0.8	1 Mbit	4 Mbit	1983	1988-89	1994
0.5	4 Mbit	16 Mbit	1986	1991-92	1997
0.35	16 Mbit	64 Mbit	1989	1994-95	2000
0.25	64 Mbit	256 Mbit	1992	1997-98	2003
0.15	256 Mbit	1 Gbit	1995	2000-01	2006

SOURCE: MOTOROLA INC.

The memory shortage of the past several years has helped Motorla's efforts, of course, since it provides a seller's market for dynamic random-access memories. But the proof is in the pudding, and now Motorola has shown that it can turn out state-of-the-art 1-Mbit DRAMs in growing volume at its plants in Austin, Mesa, Ariz., and East Kilbride, Scotland. The DRAMs are based on designs from Toshiba, the world leader in memory production; the two companies make a million 1-Mbit DRAMs per month at their joint facility in Sendai, Japan.

When it comes to fast static RAMs, which computer makers continue to gobble up as quickly as they are produced, Motorola's own design technology is key. Its latest SRAM offering, a 256-Kbit 20-ns chip, is now at the sample stage.

Motorola has come a long way since late 1985, when plummeting prices caused by DRAM dumping in the middle of a chip recession forced it to quit the DRAM market entirely. The Schaumburg, Ill.-based semiconductor giant doesn't break down its sales figures by product line, but Adam F. Cuhney, a financial analyst at Kidder, Peabody & Co. Inc. in San Francisco, estimates that memories accounted for about $300 million in sales at Motorola last year. Of that total, he says, $270 million came from DRAM sales and the rest from SRAMs. The 1988 DRAM sales were entirely from dies on wafers supplied by Toshiba, but assembled, tested, and packaged by Motorola. The analyst expects Motorola to post big gains this year in both categories.

Motorola's stated goals for the memory market are ambitious. By 1994 it is aiming for close to a 10% share of the worldwide DRAM market, which is expected to reach $12 billion that year. It also hopes to gain 10% of the projected $3 billion to $4 billion SRAM market in 1994.

"Motorola has made the decision to be a big player in the memory market," says Charles M. Clough, president of Wyle Laboratories Inc., an Irvine, Calif., distributor that handles Motorola's memory chips. But the company is "not yet the strong player [it] wants to be," he says.

Motorola's initial reluctance to divulge information about its memory program no doubt stems from the beating it took in 1985. For a company that prides itself on offering a broad product line powered by its own technology, the defeat was particularly galling. "We've kept it all low-key," acknowledges Jim George, corporate vice president and general manager of the MOS Memory Division. "We've had new technologies coming out of the oven on a crash basis every year to 18 months." George points out that one reason Motorola stayed quiet for so long is that the company views its efforts through a long-range lens. "When we came back [into the memory market], we pushed a 10-year button," he says.

To date, Motorola is the only U. S. chip maker to pull off a successful reentry into the memory business [*Electronics*, April 1989, p. 28]. It had to overcome some formidable obstacles to do so. One such barrier is the very long lead time required to design and manufacture memories. When Motorola pulled out of the market in late 1985, for example, memory makers were just readying 1-Mbit DRAMs for introduction—those chips had been in development since 1980. Development of the 4-Mbit chips now appearing in small quantities was well under way in 1985, and work was just beginning on the 16-Mbit DRAMs that will debut in 1991–92. Lead times for SRAM development are similarly lengthy. "It's a technology treadmill," says Bud Broeker, director of operations at the division. "When we jumped back in, we had to run even faster than the treadmill moves, and we're still doing it."

But Motorola had no choice but to get back into the memory business to protect its leadership position in microprocessors, says Cuhney of Kidder Peabody. He says many processor buyers, especially the smaller ones dealing with distributors, demand a package deal—with memory included. "If Motorola wanted to stay a microprocessor company, it had to have memory," Cuhney says. (Intel Corp. linked up with South Korea's Samsung

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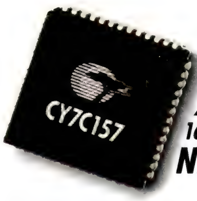

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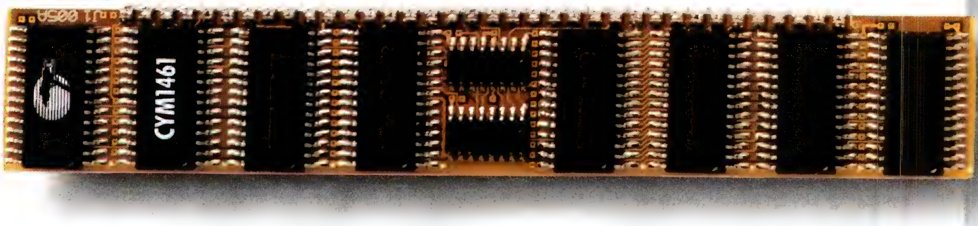

preeminent company lagging behind Sun in work-station market share.

In the aftermath of the merger announcement, top executives at both HP and Apollo spoke glowingly of joining forces. "Both companies are recognized for technical innovation and high-quality computer products, and for a commitment to the industry's move toward cooperative computing environments based on open industry standards," says John A. Young, HP's president and chief executive officer. For his part, Apollo chairman and CEO Thomas A. Vanderslice says that HP's "commitment to the work-station business and to open industry standards, its product strengths, and its well-known concern for its people add up to a very good fit."

Perhaps Apollo's most important contribution to the deal is its strong installed base of more than 93,000 work stations used by "customers who are happy with their products and technology," says Richard Watts, director of marketing for HP's Computer Products Sector. Another asset is Apollo's strong presence in electronic design automation, including the software technology contributed by its leading customer, Mentor Graphics Corp. in Beaverton, Ore.

SIZE AND STABILITY. Watts also cites Apollo's Network Computing System approach to distributed work-group computing and its RISC architecture, first introduced in the Series 10000. HP had already become a licensee for the networking software, he says, "but now we get access to that technology ahead of everyone else." In return, Watts says, HP lends Apollo size, stability, and financial resources sufficient to relieve the anxieties of its customers. Some of them were worried about Apollo's financial condition as revenues sagged and profits shrunk or disappeared in recent quarters. "We think we can put customers at ease about that," Watts says.

Most industry analysts assess the acquisition as a good one for both sides, despite the problems stemming from product-line overlaps. As for morale at Apollo, Gallup at least sounds upbeat. He says that the odds "are about a million to one that we would have been acquired by someone as well suited to us as HP is."

But an elegiac note was sounded by Apollo cofounder David Nelson. "From a founder's point of view, the assimilation of Apollo's identity into HP is somewhat disappointing," says Nelson, who recently resigned as vice president and chief technical officer to start his own company, Envision Systems Inc. in the Boston area. "It's not the final chapter we all would have written." *–Lawrence Curran*

MANAGEMENT

THE CHANGING STYLE AT SEMATECH

WASHINGTON

In the weeks after the management shakeup that left Sematech's chief operating officer, Paul Castrucci, walking the streets of Austin, Texas, in search of a job, critics of the chip-manufacturing consortium came out in full force, pointing to the incident as proof that U. S. companies couldn't work together. But officials both inside and outside Sematech say that's not the case at all—that the sudden firing of Castrucci was neither a comment on Sematech's progress nor a surprise move.

Now Sematech is on the verge of a major management reorganization that will probably result in a much more active role for chief executive officer Robert Noyce, who joined the consortium last summer ostensibly to play Mr. Outside to Castrucci's Mr. Inside. In the coming months, Sematech insiders say, Noyce may well do away with Castrucci's position altogether, replacing the single operations officer with a corps of deputies focused on specific parts of the Sematech puzzle, all reporting directly to the CEO.

Under the original plan, Noyce was supposed to have been a cheerleader and politician, handling Sematech's interface with industry and government; Castrucci was to have run the facility day to day. But that's not the way it turned out. "There were too many cooks in the kitchen," Castrucci says. "[Noyce] was around more than we expected."

The reason? Says C. Scott Kulicke, a Sematech board member and the chairman of Kulicke & Soffa Industries Inc., a semiconductor-equipment concern: "Bob Noyce is too qualified to be just a cheerleader. He's involved right up to his nose." Kulicke acknowledges that the Sematech management structure may not have been the ideal choice. The fact is, he and others say, Sematech may just be too small to support both a chief executive and a chief operating officer.

Now, with Castrucci out and Turner Hasty, a 30-year chip research veteran from Texas Instruments Inc., acting in his role, Noyce is expected to play with the management structure. Hasty, who has been with Sematech since its inception in September 1987 and who has already put in one four-month stint as interim COO, says he would "have no problem moving back into the ranks again" if that's what Noyce asks.

Is Sematech just too small to support both a CEO and a chief operating officer?

Meanwhile, Castrucci says he could tell "right from the start that the chemistry between Bob and me wasn't that good." Nonetheless, he says he was completely surprised when Noyce called him to a breakfast meeting March 20 and asked him to quit. He says his management team had met each of the goals it set in his first six months on the job, including getting the wafer fab up and running before the end of March.

"With time, I'm sure things would have worked themselves out," Castrucci says now. "Just look at the record. The fab got built. We ramped up the staff from 45 to over 500 people in six months. Wafers got processed. We got negotiations started with outside vendors [to develop advanced processing equipment]. It wasn't because things weren't getting done."

But getting things done was apparently harder than it needed to be. "What you're not looking at is the amount of effort it took to get all that work done," says Kulicke. "Differing management styles are a substantive problem."

Indeed, the problems boil down to differences in management and personal style. Noyce, a cofounder of chip giant Intel Corp., came from the free-thinking entrepreneurial environment of Silicon Valley; Castrucci arrived fresh from 32 years as a loyal IBM Corp. soldier. Noyce favored a participatory style of management, while Castrucci did things the IBM way: assign tasks, assist where possible, and wait for results to be reported back.

For some outside observers, Castrucci's departure has ominous implications. He is "a damned good manufacturing guy," says Charles Minnihan, a retired vice president from Perkin-Elmer Corp. now working as a consultant. "He's probably started more new products than anyone else in the world. This blows my mind. It really sets [Sematech] back."

Now the day-to-day management job falls to Hasty, who is currently working on signing up companies to develop the next-generation equipment, materials, processes, and test-chip demonstration vehicles for the 0.5- and 0.35-μm phases of Sematech's research program. That's the line width needed to produce a reasonably sized 64-Mbit dynamic random-access memory. The first of the contracts should be awarded by early May, with others coming over the rest of the spring and summer. *–Tobias Naegele* requires a high-end parallel-processing computer.

"We can do real-time compression in the same box that's doing the playback," says vice president John Music. Although Universal Video has publicly positioned its VP-2000 video work station directly against DVI, a third-party developer familiar with both systems is not so sure. While DVI produces full-motion video at 30 frames/s, the VP-2000 "is designed to do 10-frame/s video," says David Dering, president of American Helix Corp., a Lancaster, Pa., software developer that used the VP-2000 in a demonstration at the CD-ROM Conference. VP-2000 has potential, he says, and American Helix wants to develop software tools for it. But "people like to see 15, 20, or 30 frames/s." Universal's Music claims that when adjustments for flicker are made, viewers cannot discern the difference between 10 and 30 frames/s.

Meanwhile, Intel is filling in its software gap—and the acknowledged void in applications. "We're working with two companies to develop high-level authoring tools," says Bob Brannon, general manager of Intel's DVI operations in Princeton. The authoring package is set for release at the end of the third quarter and will run on Intel's 80386-based Pro750 applications-development platform. The Pro750 will ship in July, Brannon says. *–Jack Shandle*

TRANSACTION PROCESSING

WALL STREET LOOKING TO ROCK AROUND THE CLOCK

NEW YORK, N. Y.

Life in the financial fast lane is getting faster. Global traders in markets from treasury bills to pork bellies have their eyes on 24-hour operation, and the securities and commodities exchanges that handle the transactions are girding for fierce competition to be first to deliver round-the-clock service.

OLTP vendors scramble to give traders 24-hour service

Brokerage houses desperately "need a way to involve ourselves with the markets all around the world and pivot them around New York," says Joseph Macchia, vice president for communications at New York-based Liberty Brokerage Inc. The implications for the electronics industry have a distinctly green glow, especially for systems houses that sell on-line transaction processing mainframes and minicomputers. Stratus Computer Inc., a Marlboro, Mass.-based maker of OLTP systems, expects the exchange-automation market to grow at a 40% clip each year through the early 1990s, according to Mark Smith, director of financial services marketing.

Other technologies also stand to thrive in the push toward 24-hour global trading services. For starters, exchanges will need to upgrade their wide-area networking systems. Then too, the emerging trader's work-station market will become a battlefield for faster, smarter personal computers. There will even be a growing need for artificial intelligence applications, particularly in object-oriented programming.

Round-the-clock global trading will require more than just upgrading equipment. A major challenge is the conversion of securities clearing and settlement systems from overnight batch operations to on-line operations. "The move from 100% batch to an on-line environment is not just a matter of buying new equipment," says Smith. "The only way to handle on-line settlement is relational data bases, and they have just started to appear in on-line

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evaluation of the concept, Mandell says. "We are now in the process of filling in all the functionality," he adds.

Key to Lisp's rapid prototyping capacity is the ability to incrementally compile lines of new code without having to compile the entire program. Also, a library of about 15,000 object-oriented subroutines can be plugged in with a high probability that they will not have to be altered.

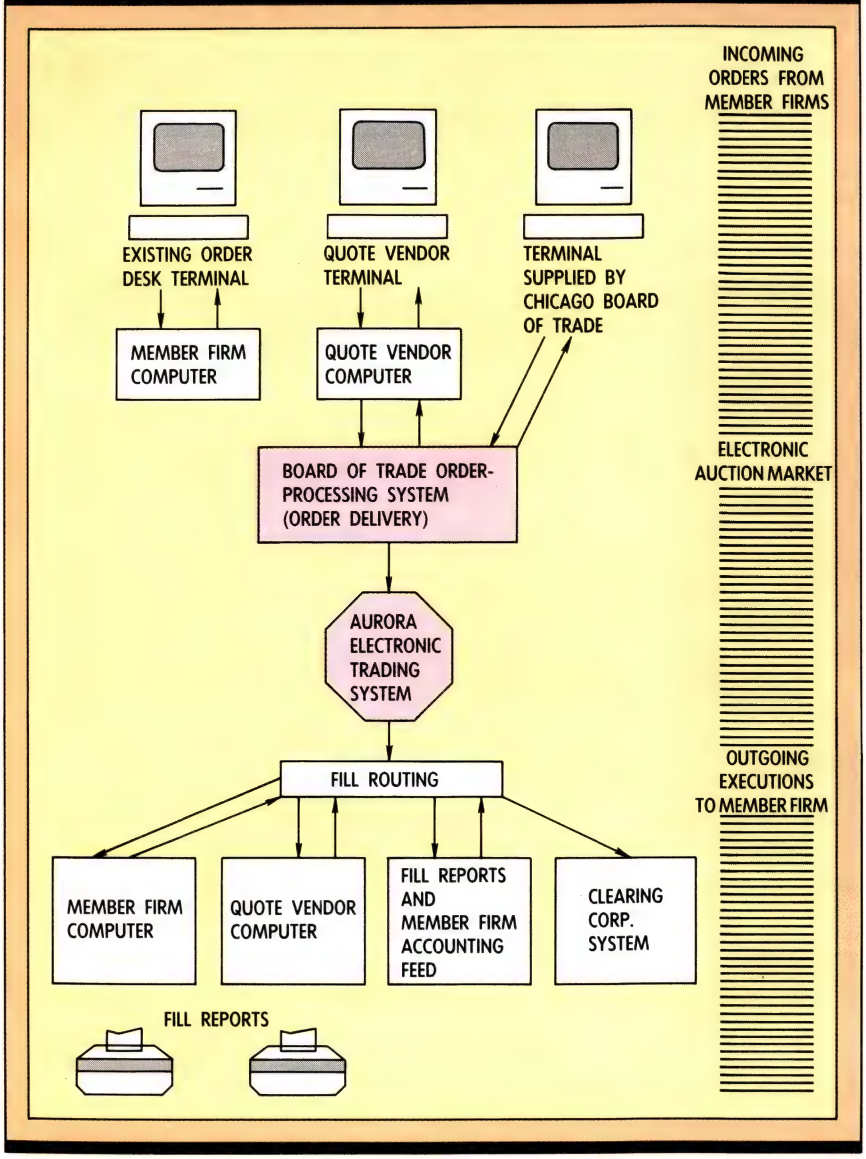
NATURAL LANGUAGE. Finally, the ability of Lisp to handle natural-language inputs is critical. "You can develop similar functionality in conventional programming languages," says Mandell, "but it's more like writing the program in stone. If you want to change something, you have to chip away at a corner and run the risk of breaking the stone."

In a another manifestation of the need for highly flexible, quick-change technology, the CBT is using Tandem's top-of-the-line VLX mainframe, which can be scaled up by adding processors as needed without reprogramming. A VLX with four processors can execute 7.5 transactions/s, says Ray Villareal, Tandem's assistant to the senior vice president for sales and marketing. Other vendors, notably Concurrent Computer, Digital Equipment, IBM, and Stratus, are also vying for the exchange-automation market for 24-hour global trading.

Among the qualities Villareal sees as crucial for this market are processor modularity, the ability to place mainframes in remote sites without on-site service, and the ability to switch computing resources from region to region as financial activity changes in time zones.

A second tier of requirements, says Villareal, includes maintaining data integrity, a feature that involves not just redundancy but also assuring that bad data, when it crops up, is not passed around the network. *–Jack Shandle*

TRADERS OF THE ELECTRONIC PIT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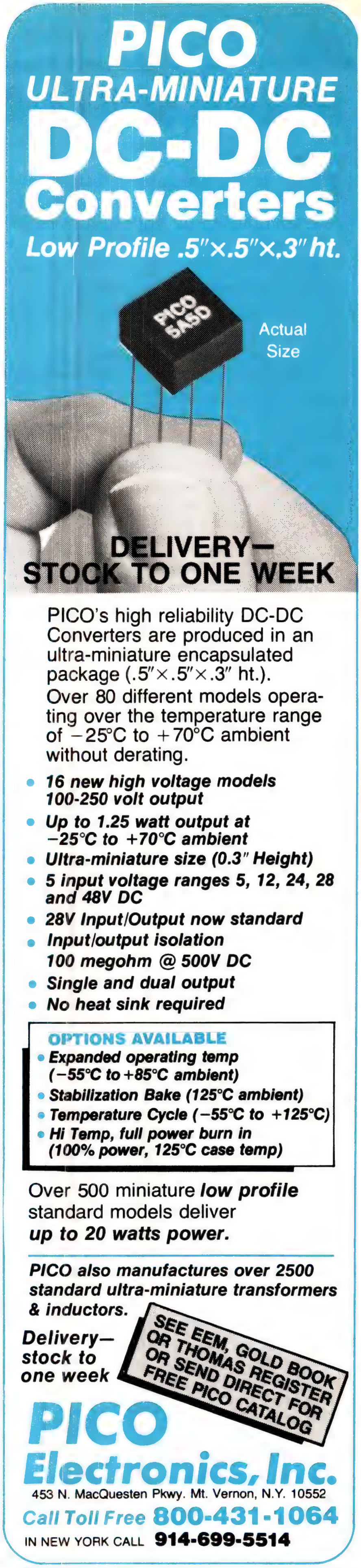
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DT2862-60Hz[4] w/ DT2858[6]	Frame Grabber & Frame Processor	512 x 512	256	8[1]			8-bit or 16-bit[2]	√[4]
DT2862-50Hz[4] w/ DT2858[6]	Frame Grabber & Frame Processor	512 x 512	256	8[1]			8-bit or 16-bit[2]	√[4]
DT2861-60Hz[4] DT2861-50Hz[4]	Arithmetic Frame Grabber	512x512	256	8[1]			8-bit	√
DT2861-60Hz[4] w/ DT2858[6]	Frame Grabber & Frame Processor	512z512	256	8[1]		√	8-bit or 16-bit[2]	√
DT2861-50Hz[4] w/ DT2858[6]	Frame Grabber & Frame Processor	512x512	256	8[1]		√	8-bit or 16-bit[2]	√
DT2851-60Hz[4] DT2851-50Hz[4]	High Resolution Frame Grabber	512 x 512	256	8[1]		–	4-bit	
DT2851-60Hz[4] w/DT2858[6]	Frame Grabber & Frame Processor	512 x 512	256	8		√	4-bit or 16-bit[2]	
DT2851-50Hz[4] w/DT2858[6]	Frame Grabber & Frame Processor	512 x 512	256			√	4-bit or 16-bit[2]	
DT2853-60Hz[4] DT2853-50Hz[4]	Low Cost Frame Grabber	512 x 512	256			–	4-bit	
DT2853-SQ-60Hz[4] DT2853-SQ-50Hz[4]	Low Cost, Square Pixel Frame Grabber	512 x 512 Square Pixel Option	256			–	4-bit	
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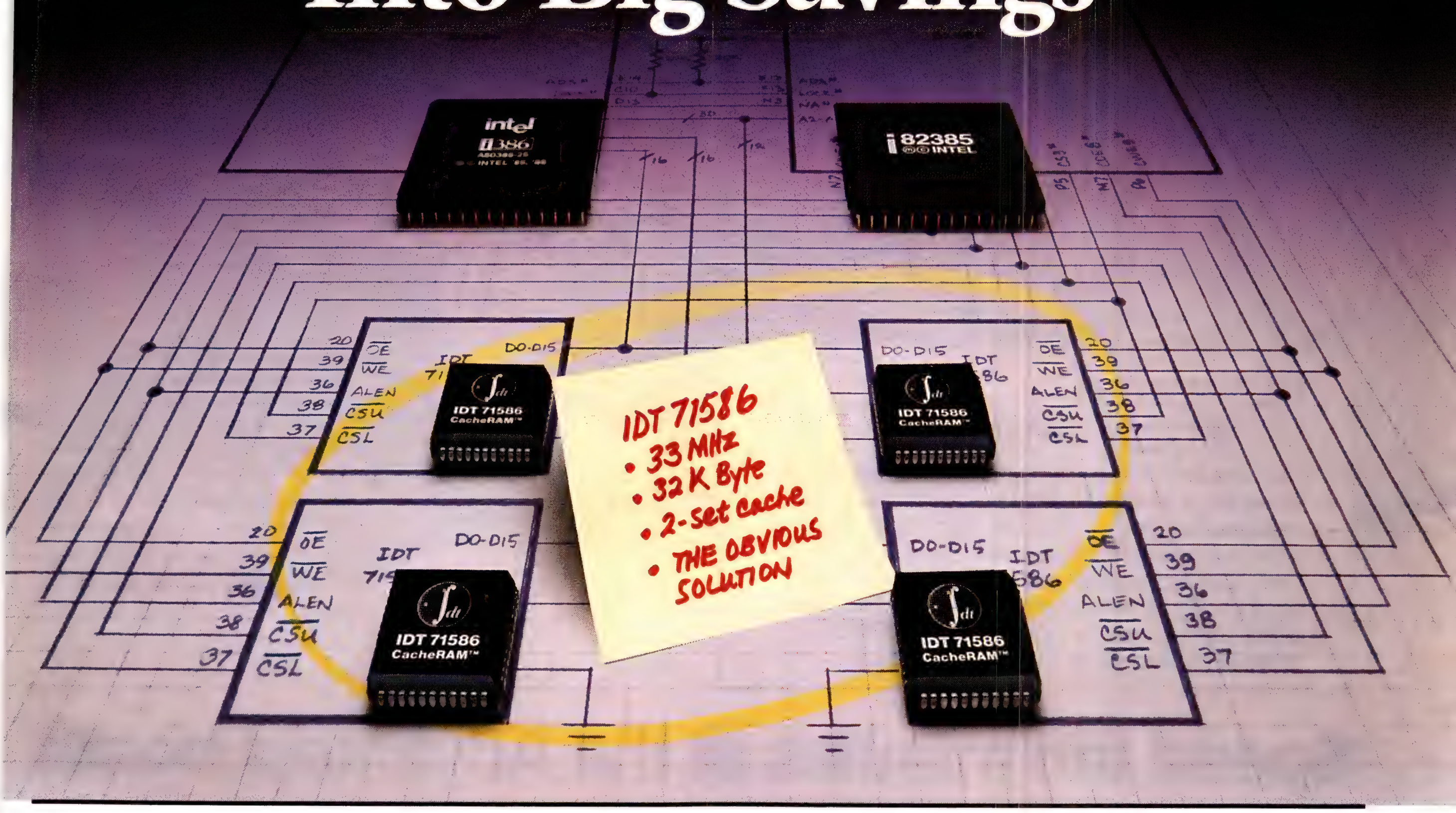

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ters the required specifications, and the system creates and simulates a draft design with a known configuration. Then a performance-suitability level is derived using the fuzzy-logic rule base. If the specs are not met, the rule base is modified until they are, on the known design. The debugged rule base is then used to design and simulate the new circuit. The loop is repeated for each of the specifications until all are met within the designer's predetermined limits.

SIMPLIFY DESIGN. Taking another path to analog design simplification, researchers at General Electric Co.'s corporate research and development center in Schenectady, N. Y., have devised a floor-planning algorithm strictly for analog circuits. Although several such techniques have been proposed in the past, all have had the unfortunate byproduct of lengthening the design cycle. But the GE method, based on the standard leaf-cell approach used in many of the digital methodologies, simplifies design and reduces design time as well.

Unlike the standard leaf-cell approach, in which sensitive and insensitive sides of each leaf are adjacent to one another, the analog leaf cells are arranged so that the sensitive sides are adjacent. This serves to form sensitive and insensitive channels. The sensitive are used for analog signal and power routing and the insensitive for digital.

OEMs are bumping up against a fact of life: the real world is analog

Researchers at Carnegie-Mellon University in Pittsburgh are taking an even more comprehensive approach to the problem. Scientists in the department of electrical and computer engineering have created a design system called Acacia that automates the entire design path from specification to silicon for critical analog modules. Its proprietary interface allows analog designers to explore various circuit trade-offs automatically.

Two of Acacia's most important components are tools called Oasys and Anagram. Oasys provides a general framework for hierarchical synthesis of circuit schematics from performance and process specifications; it's also a synthesis tool incorporating knowledge of CMOS operational-amplifier and comparator design. At any level in the hierarchy, a set of block-diagram topologies is available, and heuristics are used to select the best approach. Oasys then employs approximate analytical equations to refine the block specifications into specs. It also incorporates algorithms for automatically generating schematic drawings.

The second tool, Anagram, transforms device-level schematics into mask geometry and operates like a digital macrocell place-and-route system. The macrocells can be individual devices, such as transistors and capacitors, or groups of devices with special matching requirements, such as differential pairs, matched switches, and large folded devices. Anagram places these blocks using an annealing algorithm and then routes them using a novel analog scheme that models noisy and sensitive wiring, crosstalk, shielding, and ground loops. Anagram has laid out a variety of Oasys-synthesized op amps and comparators with what the researchers describe as good accuracy—within 10% in most cases—considering the simplified device models used.

To bring automated analog design into the range of the average designer, a new CAD methodology, called Liberty, has been developed by Custom Arrays Corp. It can be implemented on a low-cost work station, much like digital design. The Sunnyvale, Calif., company's package consists of five modules: a schematic design-entry package, a Spice simulator, an interactive symbolic layout-design editor, a mask-pattern generator, and a proprietary logic-verification routine called Decorus, which supports design-rule and electrical-connectivity checking plus post-layout netlist extraction and schematic back annotation.

Still, as important as automating the analog portion of a design is, it comes to naught if it can't be merged at the chip level with the digital portion. But design of analog and mixed-mode analog/digital application-specific ICs has lagged behind pure digital.

For one thing, analog performance is much more sensitive to the manufacturing process, says Edmund Chung, a researcher at Silicon Compiler Systems Corp. in San Jose, Calif. Then too, modeling analog circuits requires much greater accuracy than digital. Unlike digital ASICs, semicustom analog designs need elaborate characterization of the analog cells and frequent layout tweaking.

One approach to this problem comes from researchers at IMP Europe Ltd. in Swindon, UK. It makes use of so-called personalized cells, which are introduced to fit the specific needs of a design. Also factored in are layout-dependent circuit features that locate crosstalk, analog and digital noise, parasitic resistance, supply buses, and grounding.

Meanwhile, from the IC Design Center at the University of Hawaii comes a technique for constructing analog cells to be used in mixed analog/digital designs based on a technique reminiscent of the spreadsheet programs used in business. Applicable to both CMOS and biCMOS and scalable to below 1 μm, the technique is based on the tiling of modules using an internally designed layout editor. The editor incorporates a generic layout rule set that allows conversion between different mask rules and includes rules for two lay-

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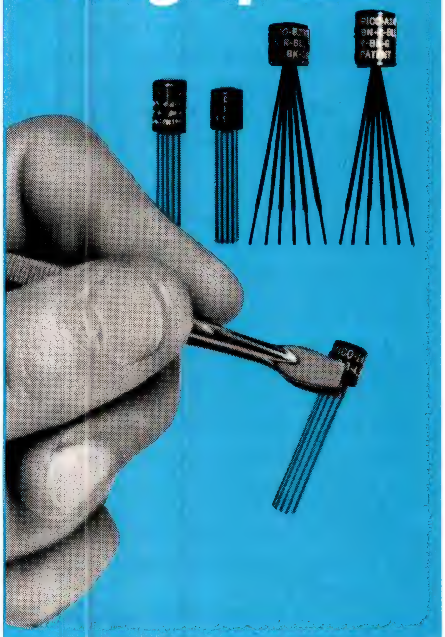

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Circle 207

ZEISS: AT THE LEADING EDGE IN LEIPZIG

LEIPZIG, EAST GERMANY

In the words of a West German industry analyst, "High technology is not the sole domain of the West. In some measure, it's in evidence in Eastern Europe too." One need go no further than East Germany to find proof of that contention: specifically, in 1-Mbit dynamic random-access memories using 1.0-μm CMOS technology. They come from VEB Carl Zeiss Jena, which aims to put the devices into production this year.

This state-owned firm—VEB stands for the German words for people-owned enterprise—has also developed sophisticated equipment for making the DRAMs. It is now planning 4-Mbit versions using 0.8-μm structures.

Of course, Zeiss Jena can't be called a typical East German, let alone East European, firm. It's in a class by itself in the Eastern bloc. But as such, it's the pacesetter for East German microelectronics, so Zeiss Jena is showing the way in which that nation is headed technologically.

With a 142-year tradition in manufacturing optical equipment, the Jena firm sells its wares worldwide, in both East and West. Of late, it has developed a strong capability in microelectronics and related production equipment, some of which has even been shipped to Japan.

Significantly, Zeiss developed the 1-Mbit DRAM samples on its own. Unlike some Western European and U. S. chip makers, it has no access to Japanese high-density-memory technology through know-how exchange or licensing agreements. For a company in the Soviet bloc, such access is restricted for competitive—not to mention political—reasons.

An important tool in the DRAM development effort is Zeiss's electron-beam exposure system, ZBA21. Used for VLSI mask making, direct exposure of wafers for quick-turnaround parts, and personalizing gate arrays, the system produces lines whose smallest resolvable width is 0.2 μm. The practical resolution under production-line conditions is 0.5 μm.

Zeiss Jena is building 1-Mbit DRAMs and plans to move up to 4 Mbits

Knut Kaschlik, director of the firm's equipment R&D, ranks the ZBA21 among the world's top e-beam machines—on a par with similar systems from Perkin Elmer Co. in the U. S. and Japan's Jeol. Western observers at the Spring Fair in Leipzig last March, where the model was shown, concur in this assessment. One model 21 user is the Soviet Union.

Zeiss had no choice but to develop the e-beam equipment on its own if it wanted to make high-density DRAMs. True, Czechoslovakia's big electronics combine, Tesla, has an e-beam system, the BS600. Advanced though it is, it doesn't meet the tough production-line requirements for 1-Mbit DRAMs.

Like its predecessor, the ZBA20, of which 70 have been sold since the early 1980s, the ZBA21 uses vector-scan deflection principles, a stop-and-go wafer- and mask-displacement scheme, and a rectangular e-beam with a variable cross-section. Zeiss pioneered this programmable-shape beam concept in the late 1970s.

The model 21's big advance over its forerunner is the increased stability of its accuracy parameters, something that helps raise device yields. The stitching accuracy of arrays for a chip measuring 9.6 by 9.6 mm is ±0.15 μm, an accuracy obtained with a 99.5% statistical certainty. Likewise, the registration accuracy checks in at 0.15 μm, also with a statistical certainty of 99.5%.

The ZBA21 also advances system productivity over that of its predecessor by optimizing specific processes and taking certain time-saving measures. For example, the beam-control data is fed from the computer-aided design system for the chip directly to the ZBA21's 16-bit control computer. This process eliminates the intermediate step of putting the data on magnetic tape.

Productivity is impressive. In one hour, the ZBA21 processes two 4-in. silicon wafers with an integration level equaling that of a 1-Mbit DRAM and with surface area fully utilized. It processes two masks per hour with 5 : 1 dual reticles on 5-by-5-in. glass, again with a 1-Mbit DRAM complexity.

Like the ZBA20, the 21 can produce lines inclined at a 45° or 135° angle at the same speed at which it writes lines parallel to the chip's horizontal and vertical axes. This is done with a turn lens that electromagnetically rotates the e-beam by 45° or 135°. Competitive systems approximate inclined lines in point-wise fashion, a slow process that tends to limit

EAST GERMANY MOUNTS A MAJOR DRAM EFFORT

East Germany's efforts in high-density memories are nothing less than its answer to Western Europe's Mega project, although the time frame for reaching the two objectives isn't quite the same.

The Mega project, a five-year Siemens-Philips endeavor that will end soon, envisions the production of 4-Mbit dynamic random-access memories and 1-Mbit static RAMs by the end of this year. But the money the East Germans are spending indicates that their aims are as ambitious as Mega's.

Of the $7.6 billion that the East Berlin government has earmarked for microelectronics research during the past several years, most went into development of the 1-Mbit DRAM samples and their 256-Kbit predecessors. The latter are now in production. These sums are hefty for a country with only 17 million people. The prime recipient is VEB Carl Zeiss Jena, an optical systems and microelectronics production-equipment maker in Jena. The company heads the country's high-density memory effort.

Zeiss is now planning the development of 4-Mbit DRAMs, already manufactures the tools for producing them, and is considering making electron-beam exposure systems needed for the 16-Mbit DRAMs of the 1990s.

One reason for the push is "the need to develop a capability for building the complex logic devices of the future," says Knut Kaschlik, director of production-equipment R&D at Zeiss Jena. Another is the Cocom list of Western technology that is off limits to the Soviet Bloc.

However, Zeiss's expertise in device technology is not limited to memories. The state-owned company has developed gate-array chips with 70,000 transistor functions and standard-cell systems with 100,000 transistor functions per chip.

Also active in microelectronics in East Germany is VEB Mikroelektronik in Erfurt. Expanding its line of 16-bit microprocessors, the company is developing a new version, the U80601, which sports a processing speed of 2 million instructions per second.

That, the firm says, is three to four times the speed of the Soviet Union's KR181o WM86, a 16-bit processor widely used in East German-made equipment. The U80601, a CMOS device to go into production in October, is part of the U80600 microprocessor system that also encompasses bus and DRAM controllers and an error-recognition and correction circuit. It is intended for multiuser and multitask computing systems. *—J. G.*

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Circle 33

that is one third less than that of its bigger brother.

The controller's early success and the continuing interest that data-processing and communications-equipment makers are showing have Siemens marketers convinced that their company will have sold about 300,000 of the 82525 and 82526 controllers by 1990. No small part in that scenario will be played by another participant in the business, Advanced Micro Devices Inc. of Sunnyvale, Calif., which will second-source the two-channel HSCX.

As is often the case with circuits that turn out to be successes on the merchant market, the controller was originally designed for Siemens' in-house use at its big Telecommunications Division. With sales of $4.2 billion last year, the group checked in as the world's third-largest producer in the field, behind AT&T Co. in the U. S. and France's Alcatel NV. But then the outside telecommunications industry became interested, and excitement was also generated among vendors of data-processing gear.

Because of its 8-bit demultiplexed adaptive bus interface, the HSCX is compatible with every 8- or 16-bit microcontroller or microprocessor system from Intel-Siemens and Motorola Inc. Siemens' evaluation boards and demonstration software, Reith says, drastically reduce design-in times—typically, to six months to a year.

The controller is suitable for a wide range of applications. The two-channel 82525 should find uses in terminals, medical patient-monitoring equipment, computers employed in telephone exchanges, and ISDN-capable personal computers. The one-channel 82526 is good for monitoring and controlling functional units in such equipment as laser printers, industrial controls, and telephone exchanges. Three applications—telecommunications equipment, nonstandard local-area networks, and general point-to-point HDLC interfaces—will each account for about one third of the sales, Karmazin predicts.

With derivates of the HSCX, Siemens wants to be prepared for future applications. On the drawing boards is a version with a bus 16 bits wide that can transfer data at a rate of 10 Mbits/s. It is suitable for synchronous and asynchronous operations. *–John Gosch*

TELECOMMUNICATIONS

GET READY FOR THE POCKET-PHONE BOOM

LONDON

The next big consumer telecommunications wind to blow across Europe could well be the digital pocket telephone—a version of the domestic cordless phone that can go anywhere. That's the conclusion of a study just completed for the Commission of the European Communities by consultants Arthur D. Little Co. of Geneva that looks at markets for all types of "second-generation" cordless telephones.

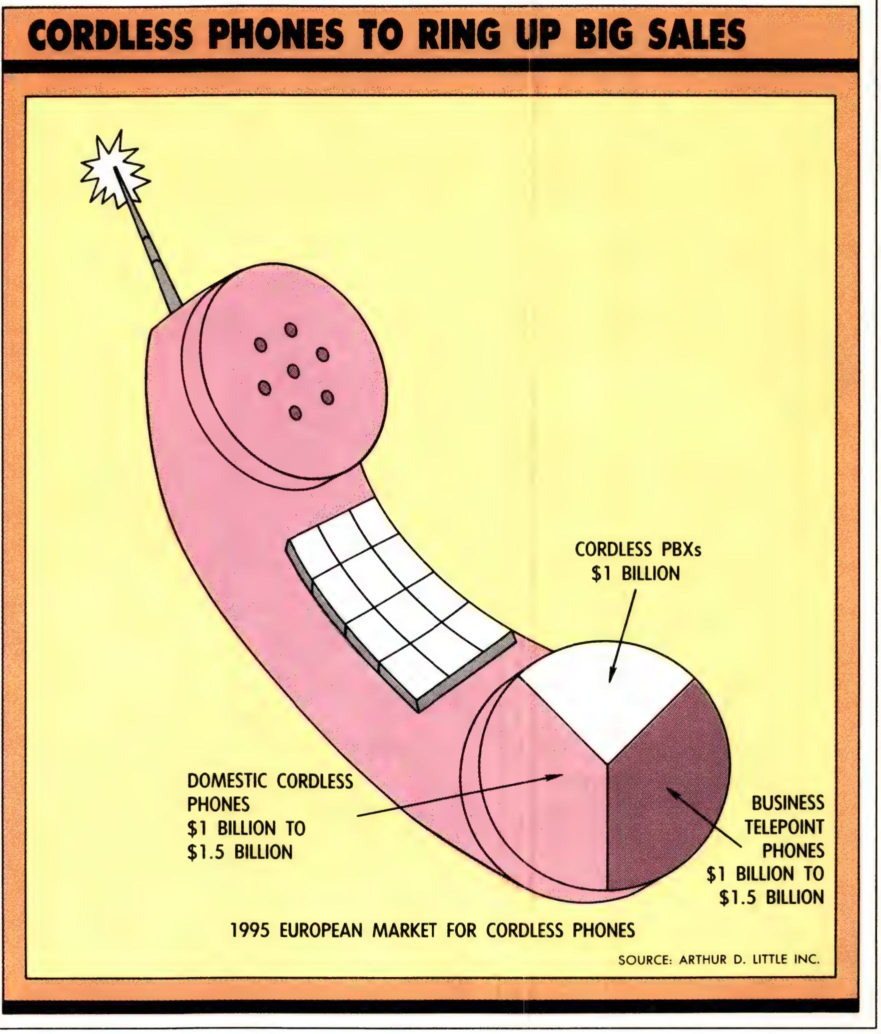
Overall, the study says, markets for cordless telephones in Europe will top $3 billion by 1995 and could reach as much as $4.5 billion. The study predicts the development of three distinct market sectors:

- Cordless private-branch exchanges for offices, which should attract an annual market of $1 billion.
- Domestic cordless telephones, a market valued at $1 billion to $1.5 billion.
- The pocket phone, or Telepoint, market. Sales to businesses could hit $1 billion to $1.5 billion, says Little, with domestic users contributing a further $20 million.

The newest sector is Telepoint, a market that does not exist now. The big question is just how fast the technology, originated in Britain, will catch on. The way the Little report sees it, pocket phones will sell as well as other domestic electronic gear, such as video-cassette recorders, provided they are priced at around $200 and conform to a common Digital European Cordless Telephone (DECT) standard.

The idea is for privately owned telecommunications companies to set up thousands of low-powered base stations, essentially the fixed half of a cordless telephone set, in strategic points around the country. Phone owners could then make calls from these stations, which will be in shopping malls, hotels, transportation terminals, and the like, and be billed at rates similar to those charged for conventional public pay phones. Earlier this year, four groups gained UK licenses to operate public Telepoint services.

Now Britain's near euphoria for the technology seems to be infecting the rest of Europe, and the French, Germans, Italians, and Spanish are all eager to climb aboard. But the EC wants a common technical standard—something that even the British will not have before 1990—or the first networks will be incom-



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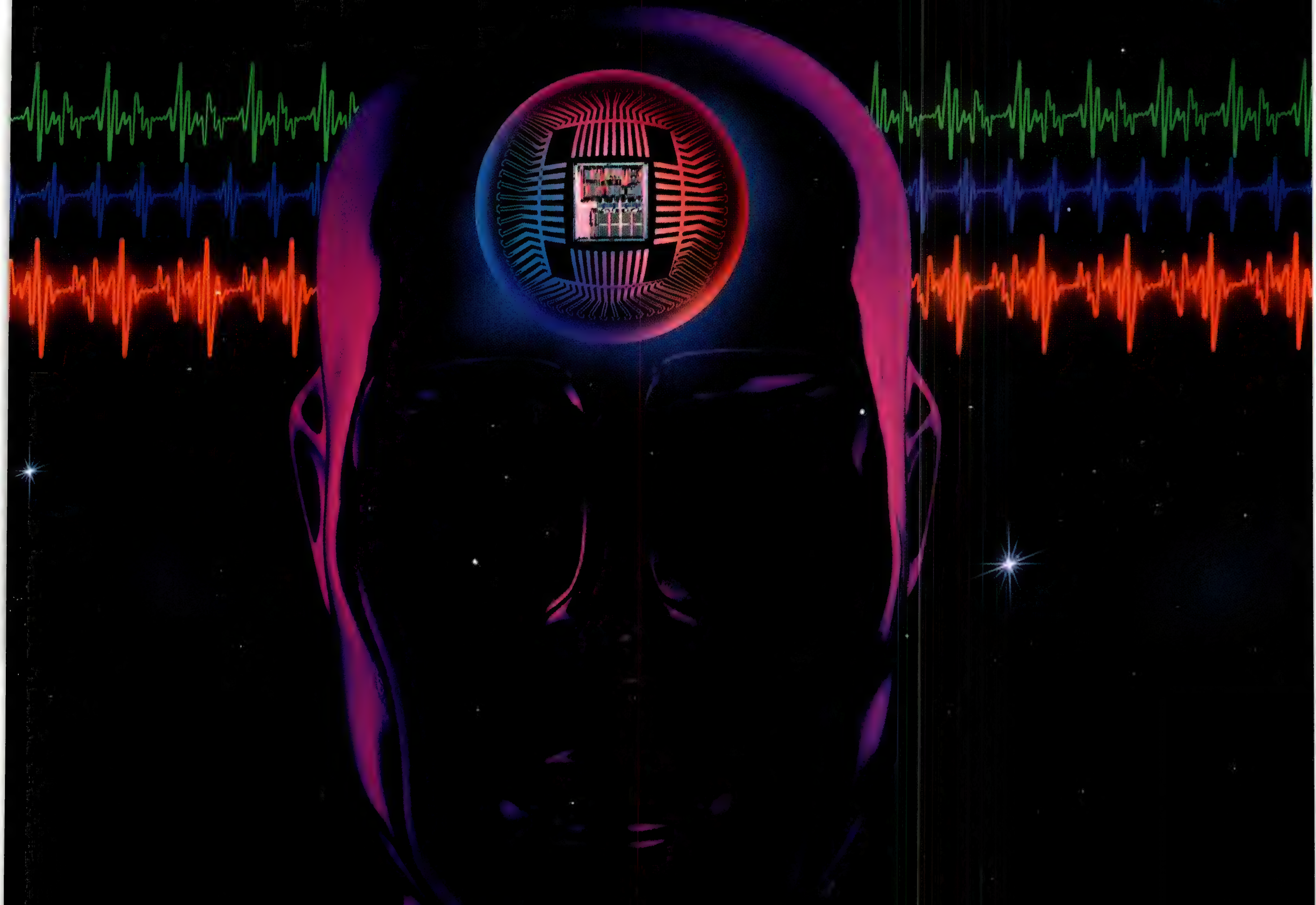

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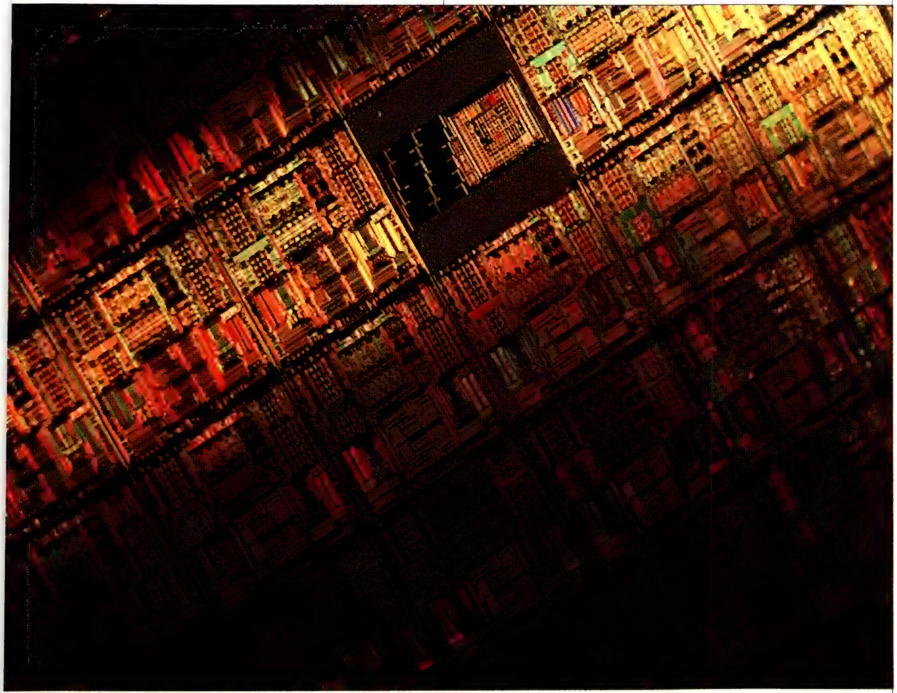

High-density Analog Interface Circuit chips demonstrate the greater integration achieved by TI's innovative linear processing technologies. These DSP interfaces allow you to alter circuit configuration under software control without external adjustments.

Advanced Linear: Intelligent power for every car

Chips fabricated with our Power DMOS-based BIDFET™ processing are replacing electromechanical relays in many automotive applications, such as driving headlamps and motors. Power BIDFET allows us to minimize power loss in the switch and add high-complexity logic functions.

Multi-EPI bipolar processing, a very cost-effective technology, is used to produce chips having inherent reverse battery protection and high operating voltages. Such chips are ideal for use in automotive antilock braking systems, electronic transmissions, and active suspension systems.

Either technology can produce devices with low-side drive, high-side drive, or H-bridge configurations.

In the future, these developments may lead to multiplexed systems for cars, replacing bulky wiring harnesses.

Advanced Linear: Enhancing modems and facsimiles

TI's dual driver/receiver is a good example of the integration achieved with advanced processing technologies. LinBiCMOS™ processing has enabled us to put the drivers and receivers needed for RS-232 voltage levels on the same chip with the charge pump required to generate the necessary split rails from a single 5-V supply. You eliminate external power supplies and get a device that's easier to design with—it is available in our LinASIC™ cell library for integration with digital ASICs.

A new family of Analog Interface Circuits (AICs) is emerging from our Advanced LinCMOS™ processing. The voice-band AICs, designed for modems and fax equipment, combine high-performance analog functions—14-bit A/D and D/A converters and switched capacitor filters—with digital functions such as control circuitry, program registers, and DSP interface. The usual clutter of resistors, capacitors, and pots is eliminated.

High-speed AICs are available for use in servo controllers and hard-disk-drive applications.

These AICs are also high-performance members of our LinASIC standard-cell library. Based on TI's proven digital ASIC methodologies, the LinASIC library has allowed us to develop complex, semicustom chips in as little as 16 weeks.

Advanced Linear: Boosting instrumentation accuracy

Even one of the most basic analog building blocks, the operational amplifier, is benefiting from TI's Advanced Linear technologies. Our Excalibur op amp family combines low power consumption with a 5X speed improvement while retaining low offset voltages. Offset-voltage drift has been cut from 300 μV to 60 μV to reduce your calibration, test, and measurement expenses.

For high-accuracy applications, Advanced LinCMOS is making possible Chopper Stabilized Op Amps with chopping frequencies 10 times higher than previously available (10 kHz). Noise levels are the lowest on the market.

The evolution in analog devices has only begun. Dramatic progress lies ahead throughout the 1990s. As the Advanced Linear leader, Texas Instruments is pledged to remain at the forefront, supplying you with new ways to link digital brains to advanced analog worlds.

For suggestions on choosing a linear supplier, turn the page.

WASHINGTON INSIDER

DARPA SEEKS TERA-OPS SPEED FROM REVAMPED STRATEGIC COMPUTING PROGRAM . . .

The Defense Advanced Research Projects Agency is now sorting through industry proposals designed to guide its Strategic Computing Program into the next generation of computer performance. "We are in the process of redirecting [the program] toward a new set of goals," says Darpa's outgoing director, Raymond Colladay, who is leaving this month to join industry. He says Darpa has "achieved the kinds of goals we set out to get five years ago"—namely, massively parallel computer designs based on standard microprocessor architectures and capable of 10 billion instructions/s. Now the agency is seeking to up the ante still further, targeting more advanced microprocessor technology, three-dimensional chip-packaging techniques, high-speed gallium arsenide digital circuits, and optical interconnects—all with the aim of getting a computer that runs a trillion operations/s. In conjunction with the National Aeronautics and Space Administration, it's also going after a nationwide distributed computing network with data rates in excess of 1 gigabit/s. "We think we realistically can achieve these goals by the mid-1990s," Colladay says. Key to the effort will be advanced chip and packaging technologies designed to squeeze the maximum computing punch into the smallest space. Hoping to boost the intelligence quotients of future missiles, aircraft, ships, and portable battlefield equipment, Colladay says, "We're shooting to get gigaflops performance in a soup-can-like volume." ☐

. . . AND FUNDS INTEL TO DESIGN 2,000-PROCESSOR COMPUTER BASED ON i860

The goal: a massively parallel computer that's 2,000 times faster than a Cray 1 supercomputer yet as simple to use as today's technical work stations. The trick: a massively parallel architecture linking 2,000 of Intel Corp.'s most advanced microprocessors, including the fast-as-a-Cray i860 [*Electronics*, March 1989, p. 25]. A full configuration, Intel says, will be capable of running 128 billion 64-bit floating point operations/s. The Santa Clara, Calif., company expects to spend $27.5 million on the project, to be called Touchstone, over the next three years, of which Darpa will contribute $7.6 million. Development will focus on system software to harness the powerful Touchstone computer; a high-speed communications network to tie all the processors together and distribute data at speeds over 100 Mbytes/s; and advanced packaging technology that will allow the prototype machine, which is due in 1991, to operate in an air-cooled environment, rather than the liquid-cooled environments used for today's most advanced supercomputers. ☐

AT THE HEART OF SDI'S ANTIBALLISTIC MISSILES LIE THE GUTS OF A PC

The microprocessor that powers an experimental antimissile weapon now under development for the Strategic Defense Initiative is the same one that runs many top-of-the-line desktop computers: Intel Corp.'s 80386. That chip, surrounded by a set of semicustom gate arrays built with Very High Speed Integrated Circuit technology, enables the Light-weight Exo-Atmospheric Vehicle developed by Hughes Aircraft Co. to process more than 100 images/s and track down a soaring nuclear missile, says Mick Blackledge, assistant director for interceptors and command control at the SDI organization in the Pentagon. The unit receives the images from a mercury-cadmium-telluride infrared focal-plane array with 128-by-128-pixel resolution. The Hughes projectile's intelligence comes from an 80386-based CPU that can calculate 4.2 million instructions/s at a sizzling 300-MHz clock rate. What's more, all that computing power fits into a 1-kg package. That's 6.3 kg lighter than the data-processing module inside the Advanced Medium-Range Air-to-Air Missile—and six times as fast. The next step? Shrinking the processor board to an even smaller 0.3 kg and forging the circuitry in radiation-hardened silicon. ☐

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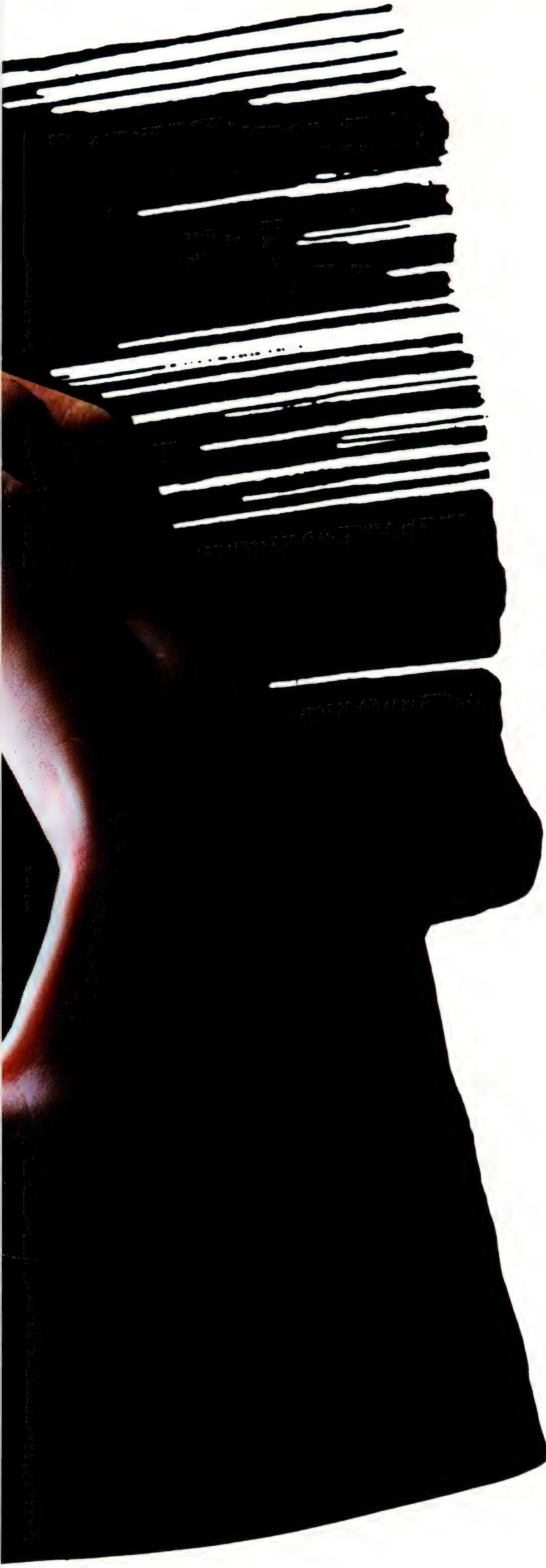


Sizing Up the Earth in 200 B.C.

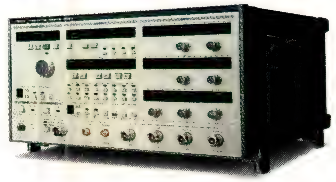
Eratosthenes believed the earth was round. As director of the great library at Alexandria in Egypt, he decided to go beyond abstract argument and actually measure it to back up the argument.

Eratosthenes

Knowing that the midsummer noon sun shone straight down a vertical well in Syene far to the south, he measured the slight angle of the sun's shadow in Alexandria on the same day. He figured the distance between the two cities by how long it took a camel to walk there. Then, with a little simple geometry, Eratosthenes came up with fairly accurate figures for the earth's circumference and radius. His pioneering measurement made a significant impact on history.

Communications Support for 2000 A.D.

Today, Anritsu's pioneering efforts in communications measurement are also paying off. Anritsu has long been a leader in the most sophisticated measuring methods, and continues to reach new levels of accuracy. The complex technologies behind modern multiplex techniques, for example, demand the highest degrees of precision. That's why carriers and manufacturers alike turn to Anritsu for the answers when it comes to accurate measuring and test equipment for communications.



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Circle 55

EUROPEAN OBSERVER

COMING: A 5-GIGAFLOPS SUPERCOMPUTER FROM WEST GERMANY

Joining the small ranks of high-performance supercomputer makers, Suprenum GmbH of Bonn has unveiled the first clusters of a system that, fully configured, will boast a computing power of 5 billion floating-point operations per second. That performance would put the machine in the class of supercomputers built by the likes of Cray Research Inc., Fujitsu Ltd., and Hitachi Ltd. The system, also called Suprenum, is the result of a four-year research and development effort at a number of West German universities, institutes, and industrial firms. Suprenum GmbH coordinated the project and is marketing the machine, which carries a $14 million price tag. The company says it has already held sales talks with 10 research institutes and universities in West Germany. Suprenum plans to extend its marketing effort to the rest of Europe next year and eventually to sell its system in the U. S. The first Suprenum clusters, each consisting of 16 processing nodes that together offer 320 megaflops of computing power, debuted at last month's Industrial Fair in Hanover. A fully configured system, slated to be available by year's end, will comprise 16 clusters, making for a total of just over 5 gigaflops. ☐

PHILIPS BUILDS A DEFENSE AGAINST TAKEOVER BIDS

Speculation about an unfriendly takeover of Philips International NV in the Netherlands should end now that the company has bolstered its defenses. The Eindhoven-based electronics giant gained some takeover insurance by altering its so-called Articles of Association agreement with its holding company, NV Gemeenschappelijk Bezit van Aandeelen Philips' Gloeilampenfabrieken—Bezit, for short. At the annual shareholders meeting last month, the authorized share capital of Bezit was doubled, from 5 billion to 10 billion Dutch guilders (about $4.74 billion). The move gives Philips a combination of priority shares and the power to issue preference shares that it can use to counter a hostile takeover attempt. The shareholders also moved to set up a foundation that will be granted an option on Bezit's preference shares to be exercised if an unfriendly takeover is attempted. There has been some speculation in the West German press that Japanese companies may be interested in taking over Philips to gain a foothold in the unified Western European market, which is scheduled to become a reality by 1992. ☐

SIEMENS ANTICIPATES A BOOM IN WORK-STATION SALES

Work stations are turning out to be one of Siemens AG's hottest items. Last year, the Munich-based company sold $54 million worth of its Sicomp WS30 work stations. That works out to more than 2,000 machines and a 40% increase over 1987 sales. Siemens expects this year's sales to increase by another 40%, thanks largely to the introduction of two new models: the Sicomp WS30-430 and WS30-450. At the heart of these machines are the MC68030 microprocessor and the MC68882 floating-point processor. Working at 25 and 33 MHz, respectively, the new systems operate at from 4 million to 8 million instructions per second. ☐

TOSHIBA TO MAKE LAPTOP COMPUTERS IN WEST GERMANY

With demand for its laptop computers on the rise in Europe, Toshiba Corp. of Japan is drawing up plans for a production facility for the machines in West Germany. The plant, expected to begin production next spring, will be located in Regensburg, Bavaria, and will be run by Toshiba Europa GmbH. Initially, the plant will turn out 5,000 laptops a month, but Toshiba expects it to be producing 20,000 machines a month by 1993. Toshiba's goal is to produce half of all the laptops it sells in Europe in Regensburg. ☐

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Multiple functions mean multiple benefits. Including much faster context switching and interrupt response, due to our compact 54-instruction set. And higher system performance, because of our fast 30MHz clock rate, 67-ns instruction cycle, and 16-bit memory mapped architecture. And our ANSI-standard C compiler is just one way the HPC family can lower engineering costs, and speed your time to market.

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HPC PRODUCT FAMILY SUMMARY

Part #	16-bit Timers	UPI	I/O	Memory ROM	RAM	Features
HPC16003*	8	Yes	32	0	256	4 ICRs
HPC16004	8	Yes	32	0	512	4 ICRs
HPC16064	8	Yes	52	16K	512	4 ICRs
HPC16083*	8	Yes	52	8K	256	4 ICRs
HPC16104	8	Yes	32	0	512	8 CH A/D
HPC16164	8	Yes	52	16K	512	8 CH A/D
HPC16400	4	No	52	0	256	2 HDLC & 4 DMA
HPC16083MH	8	Yes	52	8K UV	256	UV Emulator

Standard features: Watchdog, Synchronous Serial Peripheral Interface, Uniform Memory Address Space, UART, 32X16-bit divide, 16X16-bit multiply, and available as standard cell.

DEVELOPMENT TOOLS:

PC-based development system

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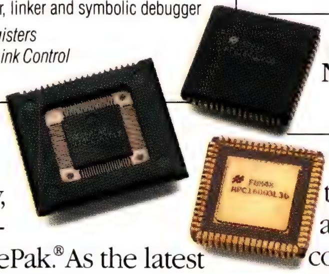
ICRs = Input Capture Registers

HDLC = High-Level Data Link Control

**MIL-STD 883C*



Another is packaging, and specifically, our unique feature called TapePak.® As the latest generation in VLSI packaging, TapePak gives you a wide variety of industry-standard, high-density, high-leadcount options. When you put it all together, then throw in eight timers and up to 11 addressing modes, you can easily see why members of the HPC family are considered smart cookies indeed.

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The HPC family has more on-chip integration, and increased I/O. And that can mean a lot more capacity to manage system functions. It can also mean a lot less, when it comes to reducing board space and chip count. In addition, our Universal Peripheral Interface (UPI) allows you to partition your system, by using the HPC as a peripheral to a host processor for high-end applications.

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For data communications, and especially for those applications requiring protocol conversion, we offer the newest member of our HPC family: the HPC16400. It's a complete solution, supported by a full library of application-specific software. With two full-duplex HDLC channels, driven by 4-channel DMA, plus one full-duplex programmable UART channel for rate adaption, the HPC16400 is completely optimized for TE, TA, and line-card applications.

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To get a free brochure on our full HPC family, call us today at 800-825-5805, ext. 100. Once you discover how we do business, you'll agree that when it comes to 16-bit controllers, there's only one company of choice: National.

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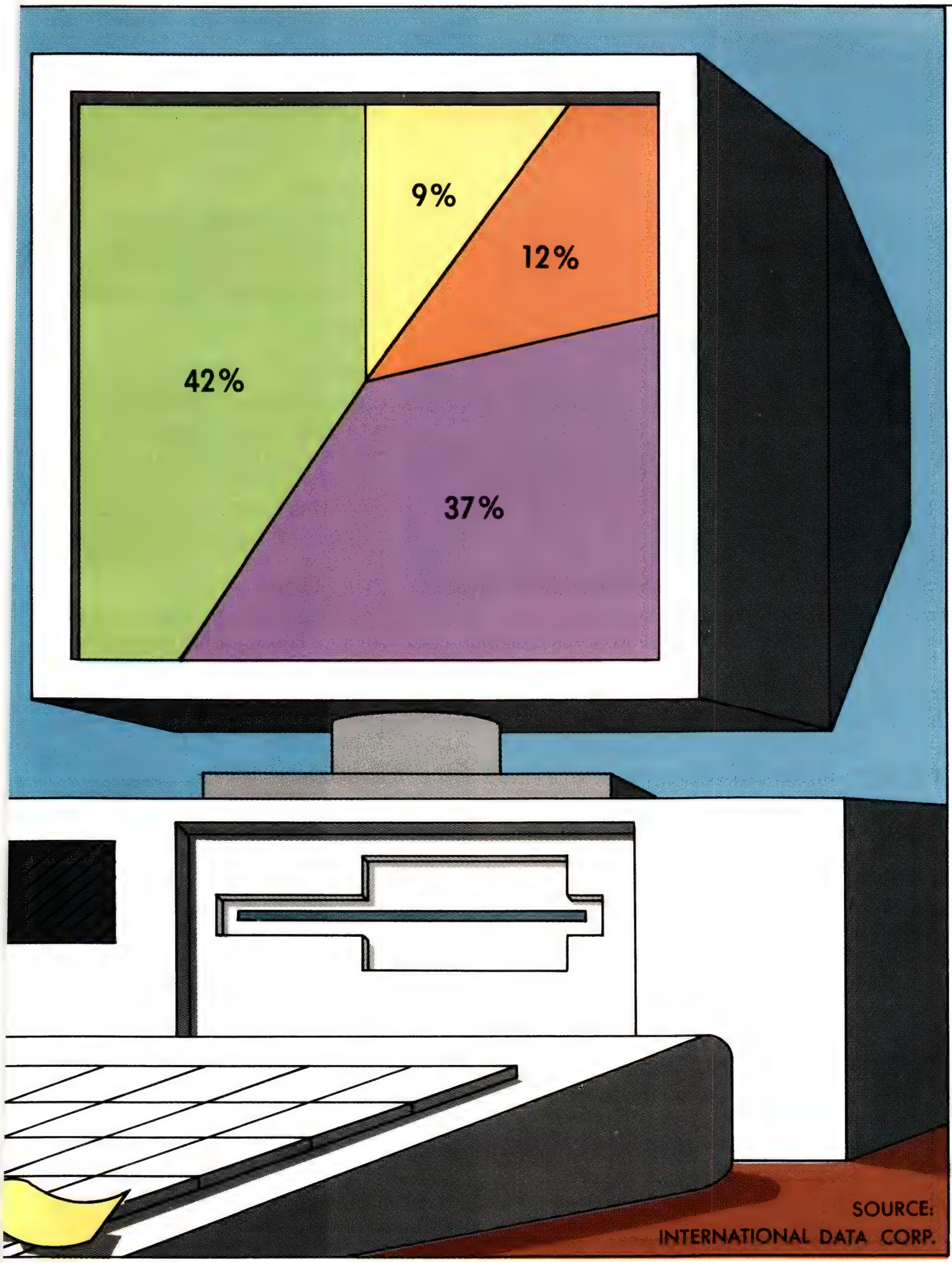
Circle 13



SOURCE: INTERNATIONAL DATA CORP.

OEM can afford to ignore. "There are around 4,000 applications written for 68020-based Unix platforms," says Travis Lutton, editor and publisher of *PC/ Workstation Wars*, a San Jose, Calif., monthly newsletter on work stations. "But only around 400 have been written for RISC-based work stations." In addition, there are 2,200 applications running under Xenix on the 80286- and 80386-based computers, says Richard Yanowich, the manager of developer relations and market development at the Santa Cruz Operations in Santa Cruz, Calif.

Both users and software developers have a vested interest in this installed base. For their part, users have a wide variety of different applications available on these CISC-based platforms. And applications developers can add more features and functions to existing software to take advantage of the increased computing power of next-generation platforms. Or they can write new programs that can sell into a large installed base of compatible systems.

Porting that software to a new platform is expensive and time-consuming, no matter how clean the new architecture or how compatible the compilers on different platforms, says Butts at Mentor. Developing and maintaining two separate sets of software starts to cost a significant amount of money after a while. Mentor's product line comprises around 5 million lines of source code; doubling that amounts to a substantial investment in programmers' time.

In addition, getting software developed for a new platform is a Catch-22 situation. Software developers are reluctant to create programs for a platform until it has a decent number of users. Users are reluctant to buy the platform until it has a respectable amount of software that can run on it.

The advantage that existing CISC chips have in software ties into the potential that opens up for them with the newer, bigger semiconductors. Using the enormous number of transistors now available and working with far more effective circuit-design tools, CISC-chip makers are creating what amounts to a new class of microprocessor: the CRISP chip.

Both Intel and Motorola's newest chips—the 80486 and 68040, respectively—qualify for the new designation. They incorporate RISC-like features to run in under two clock cycles instructions that once took four to six cycles, and they take advantage of more transistors and better design to cram onto one chip floating-point and memory-management units and caches to further boost performance. Both rival RISC chips in their power—but at the same time they are direct descendants of their CISC predecessors, and so they maintain software compatibility with them. The immense library of CISC-based applications packages is available to their users.

"Having less than two cycles per instruction on a CISC machine means that frequently executed instructions such as Load, Store, and Add are implemented in hardware rather than microcode," says Mentor's Butts. That takes more gates, of course, "but with 1 million gates possible on a chip, CISC designers have gates to spend," he says.

Both new chips incorporate an integer unit that is fully compatible with earlier members of their families. Both of them contain MMUs that first appeared on-chip with the previous-generation 80386 and 68030. However, both companies have improved the MMUs on the newer devices to up performance. For example, Motorola added two independent address-translation caches to the 68040 paged-MMU which allow simultaneous translation of both instruction and data accesses.

Both processors have on-board four-way set-associative caches. The 80486 has an 8-Kbyte shared cache. The 68040 has separate address and data caches, although Motorola will not reveal their capacity. With the MMU's address-translation caches, the independent address and data caches allow the 68040's integer and floating-point unit to access the instruction and data cache simultaneously.

That means the on-board floating point

microprocessor world is inevitable, barring the development of some unforeseen technology that will eclipse RISC, CISC, and CRISP alike. The trend is evident in the market projections people are making for the various architectures.

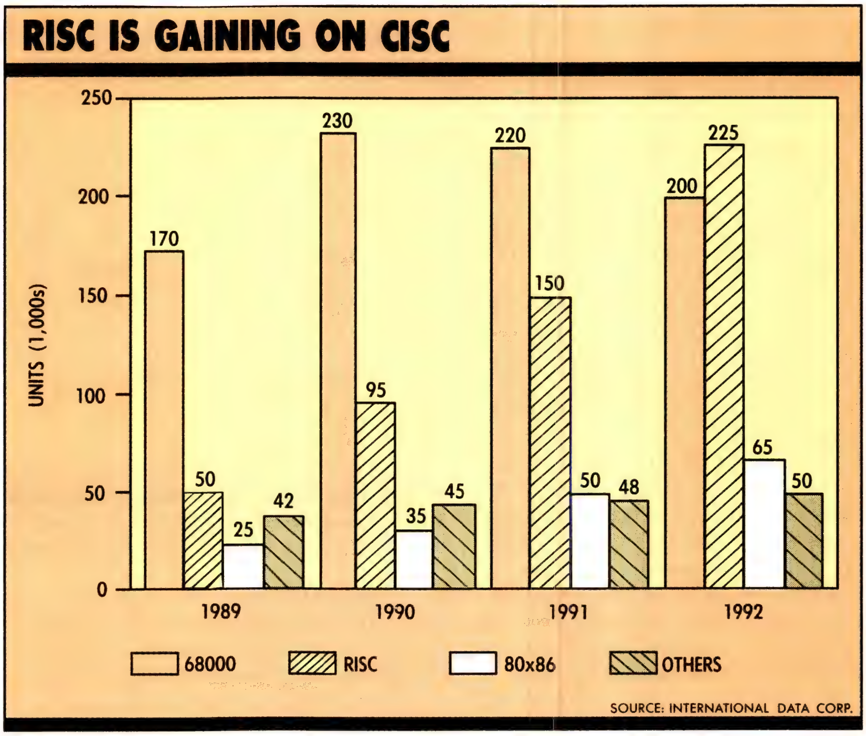
For example, International Data Corp., the Framingham, Mass., market-research firm, expects sales of all work stations to grow at a compound annual rate of over 36% through 1992. But work stations built around RISC chips will grow at 83%, from 50,000 units shipped this year to 225,000 units in 1992. Of the 540,000 work stations of all kinds expected to ship in 1992, IDC predicts 42% will be RISC-based machines, 37% CISC-based, and the rest CRISP or some other architecture.

Perhaps the greatest evidence that RISC is the wave of the future is not market figures but the actions of the market leaders. Both Intel and Motorola, the leading sellers of conventional CISC processors, have introduced RISC processors of their own. Intel's chip, the 80860, is the newer of the two, arriving a little more than two months ago [*Electronics*, March 1989, p. 25]. Motorola's 88000 came out a little more than a year ago [*Electronics*, April 28, 1988, p. 75].

A FIRST. The 80860 from the Santa Clara, Calif.-based Intel is the first RISC processor to take advantage of the chip capacity made possible by the latest semiconductor technology. Along with the 32-bit integer processor—which uses a very small set of 32 instructions—are a floating-point unit, memory-management unit, graphics processor, and cache. Connecting all of them is an extensive network of 64-bit-wide buses moving data at the rate of a gigabyte per second around the chip. Most other RISC chips have a 32-bit internal architecture.

However, Intel's competitors say the compilers for the Unix operating system are, so far, not sufficiently developed to make the chip a competitive threat. Intel announced C and Fortran compilers and Fortran vectorizers when it introduced the chip.

Nevertheless, a number of system makers have signed on to use the 860. Mercury Computer Systems Inc., a manufacturer of application accelerator boards in Lowell, Mass., is one of them. Stratus Computer Inc., a Marlboro, Mass., manufacturer of fault-tolerant computers, is another. Mercury's first products, using the 33-MHz version, are scheduled for introduction in the fourth quarter of this year, with volume shipments to begin in early 1990. Stratus is actually switching from another RISC chip, the Motorola 88000, to the Intel 860 as its central processor for a future product family to be introduced in the early 1990s.



RISC IS GAINING ON CISC

SOURCE: INTERNATIONAL DATA CORP.

> *Reports of the death of CISC are exaggerated, but if current trends continue, the future belongs to RISC*

The 88000 from Motorola, based in Austin, Texas, is not as highly integrated as Intel's chip. The 88000 actually consists of two chips, one holding the integer and floating-point units and the second carrying the memory management, cache memory, and cache logic. On the other hand, it's been around longer and hence has been designed into more systems—depending on production volumes, some 20 companies are planning 88000-based systems.

Chief among them is Data General Corp. in Westboro, Mass. The chips are being used in a 20-MHz single-processor version and a 40-MHz dual-processor version of Data General's machines.

The 88000 uses an instruction set slightly larger than the Intel 860's, but is still quite small at only 51 commands, none larger than 32 bits wide. It can execute in less than 1.5 instructions per cycle, using an architecture divided into independent execution units: the data unit, the instruction unit, the floating-point adder, and the floating-point multiplier. Each unit has its own pipeline and can execute concurrently. The companion chip provides memory-management logic, 16 Kbytes of fast-cache static RAM, and cache-control logic.

The first version of the chip set is now entering volume production. It can run at 14 to 17 mips of throughput using a 20-MHz clock. This month, Motorola will start offering samples of a 25-MHz version that will push performance up to 20 mips or more.

A number of architectural variations are also being considered. One obvious one is an integrated version, putting the processing units and the memory functions on one chip. Another is a less expensive version, without the floating-point processor, targeted at embedded processor applications (see p. 74). Yet another would be specialized application-specific variations with instruction-set extensions. Also being considered are architectural variations that incorporate expanded data, address, and instruction buses to push the execution rate faster, to under one clock cycle per instruction.

In cooperation with Data General, Motorola is also working on a multichip, bipolar emitter-coupled-logic version of the 88000. Scheduled for completion in early 1990, the new chip set would be blindingly fast: a sustained data rate of 100 mips and a peak rate of at least 140 mips.

Even higher performance will result from the ECL variant of the 80486 that will be jointly developed for a multiprocessor system by Intel and Prime Computer Inc. of Natick, Mass. However, the companies do not anticipate releasing a teger processor. No standard definition for an MMU, cache controller, cache scheme, or floating-point unit was available. And the only implementation was a gate-array version, from Fujitsu Microelectronics Inc. in San Jose of the integer processor and a floating-point controller chip for Weitek floating-point units. The MMU, cache control and configuration, and floating-point computational units were left up to the customers and the chip vendors.

There's a Catch-22 in software: developers wait until a platform has users, users wait until there's lots of software

A movement is afoot now to standardize some Sparc reference architecture definitions for these features. For example, a new implementation from Cypress Semiconductor Corp. in San Jose provides a complete architecture including the integer processor, floating-point unit, memory management, and cache, and sets up support for multiprocessing.

The multiprocessing support includes a direct-data-intervention multiprocessing protocol for maintaining cache consistency. The chip's memory-management unit conforms to the Sparc reference MMU architecture. Other reference specifications adopted include one for the module bus. In addition, Cypress is circulating the specs for its cache-consistency protocol among the members of Sparc International with the suggestion that it become a Sparc reference standard available to all Sparc licensees.

The Cypress chips—the 7C600 family—are being built using a 0.8-μm CMOS process technology, which the company claims is the most advanced CMOS in production. With this process, Cypress can produce highly integrated processor chip sets running at 33 to 50 MHz.

So far, the integer unit is rated at 25 and 33 MHz in different versions. Currently, floating-point support requires a CY7C608 floating-point controller and CY7C609 floating-point unit. But this quarter Cypress will have samples of an integrated 64-bit floating-point engine, the CY7C602, that completely implements the Sparc floating-point instruction set. The CY7C602 will be offered in 25- and 33-MHz versions delivering over 5 million double-precision Linpak floating-point operations per second.

To round out the set, Cypress is building an integrated cache controller and MMU chip in two flavors. The CY7C604 is a complete implementation of the Sparc reference MMU architecture. This chip will make Sparc the first RISC architecture to support real-time processing—it will have the capability of locking entries in the on-chip translation lookaside buffer and entries in the cache's RAM.

The second flavor is the CY7C605, which is a superset of the CY7C604 CMU that supports multiprocessing with a dual-cache-tag architecture, plus a cache model that allows each processor to access each cache directly while maintaining coherency among them. The CY7C604 will be available in sample quantities this quarter at 20, 24, and 33 MHZ; samples of the CY7C605 will be available in the third quarter at 25 and 33 MHz.

Fujitsu, the makers of the first Sparc chip, now has its second-generation implementation in production. The 25-MHz S-25 integer chip, implemented with the Fujitsu 1.2-μm CMOS process, can achieve sustained performance of 15 mips. Fujitsu also makes floating-point controller chips to go with the Sparc integer processors. It expects to ship in volume in a couple of months.

A third generation of Sparc architecture, Sparc-H, has been in the works for the past year at Fujitsu's Advanced Products Division. Samples should be available in the second half of this year. "Sparc-H is the next level of price/performance beyond the Cypress implementation," says Susan Mason, Fujitsu's marketing development manager. Sparc-H

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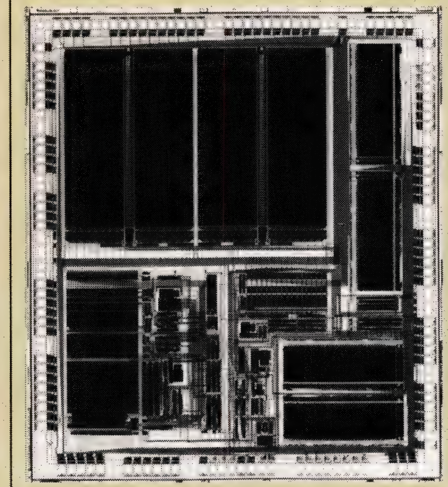
rection was the introduction in late April of sample quantities of a 32-bit RISC processor, the 20-MHz, 16-mips VL86C020.

Meanwhile, Motorola has announced that toward the end of the year it will begin offering samples of the MC68332, a high-end, 16-MHz embedded processor/controller built around a 68000/68020 core. Motorola's basic strategy is to offer an upgrade path to users of both the 8-bit 68HC05 and the 16-bit 68HC11 microcontrollers and to designers of 68000-based embedded-processing applications, says Brian Wilke, advanced MCU operations manager for Motorola.

Containing all of the 68000/68010 instructions and some of those from the 68020, the CPU core, with a two-clock bus, has a respectable 8-mips peak performance at 16 MHz. That gives it 65% to 80% of the performance of the 68020. A 16-by-16 multiply takes 1.5 μs and a 32-by-16 divide takes 1.9 to 2.5 μs.



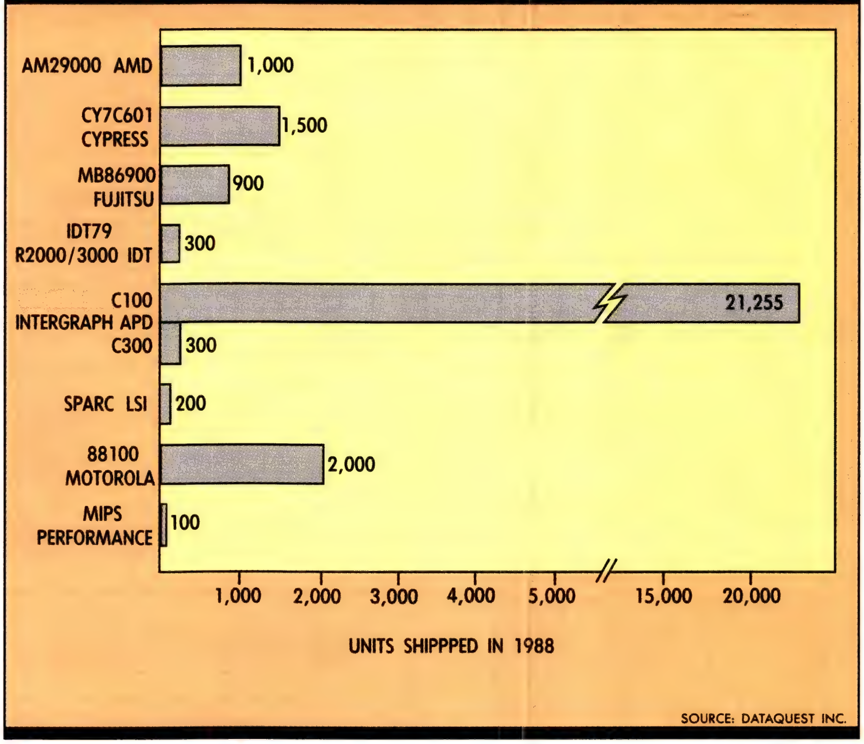
VLSI Technology's VL86C010 is the core of a set of application-specific controllers.

Coming later this year from Intel in Santa Clara, Calif., is the second generation of application-specific 80860 processors. The first device will be built around a core CPU with throughput rates up to 66 mips with only a 33-MHz clock. Fabricated in the company's 1.0-μm CMOS process, the core gets its high performance by its ability to execute up to three instructions in a single clock in most cases, and up to two instructions per clock doing time-consuming loads and branches.

The next-generation 960 core will have seven basic units: the instruction sequencer, execution unit, address generation and multiply-divide units, the local register cache, register file, and instruction cache. It will contain a three-stage pipeline for the basic ALU; a three-, four-, or five-stage pipeline for loads; and a two stage-pipeline for branches.

Although the performance of the various application-specific 860 processors depends on the environment, the company says, the core element itself has been tested using a number of benchmarks. Assuming zero wait state external memory, 33-MHz operation, and no data cache, the 860 core runs a matrix multiply at 66 mips, a copy operation at 45 to 60 mips, and a compare operation at 66 mips—speeds more than 10 times greater than the previous generation of Intel controllers. *–Bernard C. Cole*

WHO'S IN FRONT: 32-BIT RISC CHIP SHIPMENTS



SOURCE: DATAQUEST INC.

ble applications software, an independent company, Synthesis Software Solutions Inc. of Sunnyvale, was set up by MIPS a year ago to be a software services and development organization to all companies building computers out of the MIPS chip set. "Synthesis does its job two ways: by contracting to license or relicense products developed by others and, over time—within the next year—developing its own tools," says Owen Brown, the company's president and chief executive officer. Synthesis is concentrating on horizontal packages—tools and tool sets, such as compilers along with tools for optimization and porting.

The Synthesis software catalog, issued last January, contains 24 software packages distributed by Synthesis and references 48 packages distributed by other companies. Data-base systems are the dominant type of software currently available. The second most popular category is languages. Synthesis plans to expand in the next two years beyond the data-base emphasis with communications and interoperability tools and more languages, according to Brown.

POPULAR. MIPS's approach is proving commercially attractive—industry experts say 30 to 35 major computer companies are building systems around it or plan to in the immediate future. Vendors with systems on the market include Silicon Graphics Inc. of Mountain View, Calif., the leading supplier of high-performance, three-dimensional-graphics work stations, and Ardent Computer Corp., Sunnyvale, Calif., with its Titan supercomputer work station.

The biggest and best-known company to sign up with MIPS did so early this year: Digital Equipment Corp. in Maynard, Mass., introduced a series of high-end work stations based on the MIPS processors [*Electronics*, February 1989, p. 49]. Another big name, Sony Corp., has announced that it will use MIPS processors for future Sony NeWs work stations. And MIPS itself has gotten into the systems business with a line of desktop work stations.

The Sparc and MIPS architectures both are technological leaders and strong market contenders, but the market leader is the first commercially available RISC processor, the Clipper, from Intergraph Corp. in Huntsville, Ala. Intergraph, a work-station vendor, bought the Clipper technology from Fairchild Semiconductor Corp. in Cupertino, Calif., when Fairchild was acquired by National Semiconductor Corp. of Santa Clara; National already had its own RISC offering, the 3200 family. Some 20,000 Clipper chip sets have been sold.

The Clipper series—there are two products, the C100 and the newer C300—is similar in architecture to Motorola's 88000. The two processors have in common their ancestry and architectural philosophy, but diverge on the details of hardware implementation and instruction-set makeup. Unlike the MIPS architecture with its roots at Stanford and the Sparc architecture with its Berkeley origin, the Intergraph and Motorola implementations can trace their genesis to the supercomputer designs of Seymour Cray, founder of Cray Research Inc., the supercomputer market leader.

Both use register scoreboarding to allow multiple instructions to execute concurrently with a guarantee that "stale" data will never be used. Both architectures are oriented toward multiprocessing applications and therefore are partitioned similarly, with the integer and floating-point units on one chip and the cache memory and logic integrated on another chip. In both cases, a minimum three-chip set is required: the CPU and separate cache/memory-management chips for instruction and data. All data transfers to and from main memory are done via an external multimaster bus that allows multiple chip sets to share main memory.

> *The Sparc and MIPS architectures are both strong contenders, but in the RISC market, the leader is still the Clipper*

Internally, the CPUs reflect a similar philosophy with multiple execution units that operate concurrently. Both are pipelined, with three stages for the Clipper and four for the 88000.

One major advantage OEMs see in the Clipper family compared with other RISC machines, including the 88000, is availability, not just in sample quantities, but in volume production. Where the Clipper departs from the 88000 is not in its technology but in its longevity in the market.

"When we started development on our product, we looked at everything that had been announced," says one Clipper user, Dale Petros, a software engineer at Lennane Advanced Devices Inc. in Sacramento, Calif. "We found that the only real RISC machine around that was in volume production and that we could reliably depend on for parts in the quantities we needed was Intergraph's."

Similar concerns were what brought Intergraph one of its most important customers to date: E. I. Du Pont de Nemours and Co., based in Wilmington, Del. The deal allows for volume purchases of 50,000 units or more per year, which will

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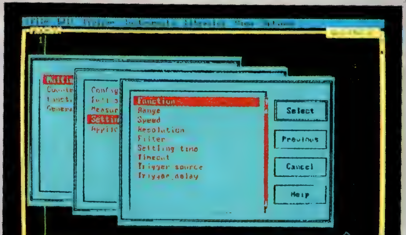

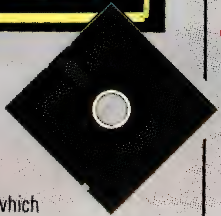

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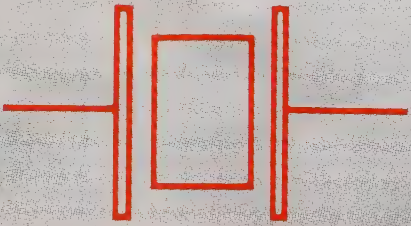
GPIB system testing oscillators



A company in West Germany has built a GPIB test system to align crystal oscillators. The system measures the frequency deviation at the crystal for various temperatures, calculates the required compensation network, aligns the oscillator and prints the resulting circuit's frequency/temperature curve within seconds. The System 21 DAC, coax switch and low level switch are used to interconnect the oscillator with the test instruments under GPIB control. Low cost and ease of connection were the principal reasons why this company chose System 21.

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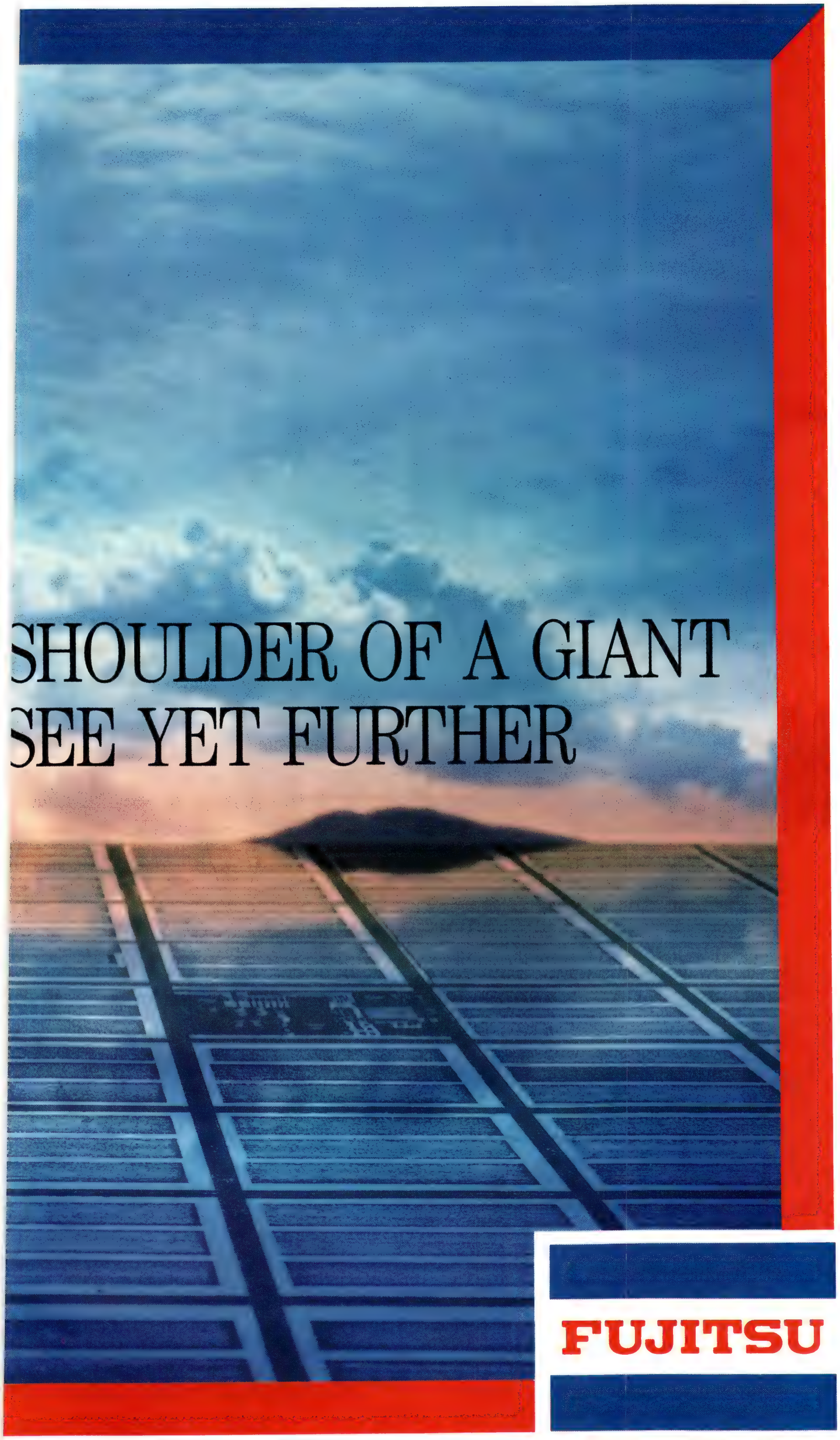

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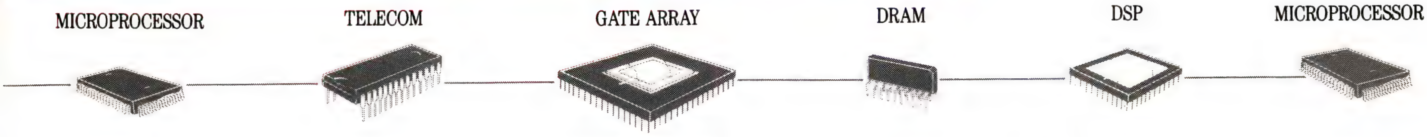

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Circle 47

nologies to the future defense of the U. S., the Pentagon ranked GaAs development second only to microelectronics advances in general.

This mixed message has already irked some congressmen and may become a topic of debate when serious discussions of the fiscal 1990 budget get under way. That debate has already started, with Darpa firing the first salvo: Roosild says the $19 million SDI is seeking for GaAs research in 1990 "is not really enough to support a program that goes anywhere."

Why has GaAs lost its luster? The answer lies primarily in the more immediate success of two alternatives—bulk CMOS silicon and silicon-on-insulator, a variant of the older silicon-on-sapphire technology that is now the most common choice for critical rad-hard applications. Experts agree that GaAs will always be tougher than any silicon technology when it comes to "total-dose" radiation—the ability to survive a lifetime of repeated exposure. This can ultimately damage the material of a chip, slowing it down and otherwise degrading performance. But the difference in yield, cost, and, more important, circuit density, have made these alternative technologies more and more attractive.

GaAs also has an edge over most silicon technologies in terms of speed, but because of the huge weight concerns of space platforms, density is often a more critical consideration. So experts now expect GaAs to be used only in niche applications, where its unique combination of speed, power, and hardness are expressly called for. "The only place GaAs is better is total dose," says Barry Dunbridge, assistant general manager for technology at TRW Inc.'s Electronics and Technology Division in Redondo Beach, Calif. "Since it's no better with the other [criteria], it simply doesn't have anything to offer. You've got to ask: do you really need the speed for the higher cost?"

So for the short term, silicon in some form is the answer. That solution seems remarkable in light of the conventional wisdom of a decade ago, when silicon MOS technologies were considered "too soft" for space and missile applications, Dunbridge says. At that time, the military and the National Aeronautics and Space Administration leaned on conventional or dielectrically isolated bipolar technologies for their nuclear and space-based missions. But as the industry shifted away from n-channel MOS to CMOS while embracing smaller and smaller geometries, designers also had to move to thinner oxide layers on their chips. In so doing, they fell upon a happy accident: once oxides were cut in half, to about 250 Å or less, it turned out that "CMOS was good enough for peaceful space applications," Dunbridge says.

Total-dose hardness levels of 100 Krads and higher were easily attainable. Likewise, as operating speeds improved, CMOS became less susceptible to dose-rate attack, a sudden blast of radiation that can cause photon-induced currents to course through a chip, causing a spike effect that can upset memory bits and cause logic transitions. Halving the oxide thickness produces a factor-of-eight improvement in total-dose hardness and a four-times improvement in dose-rate protection, Dunbridge says.

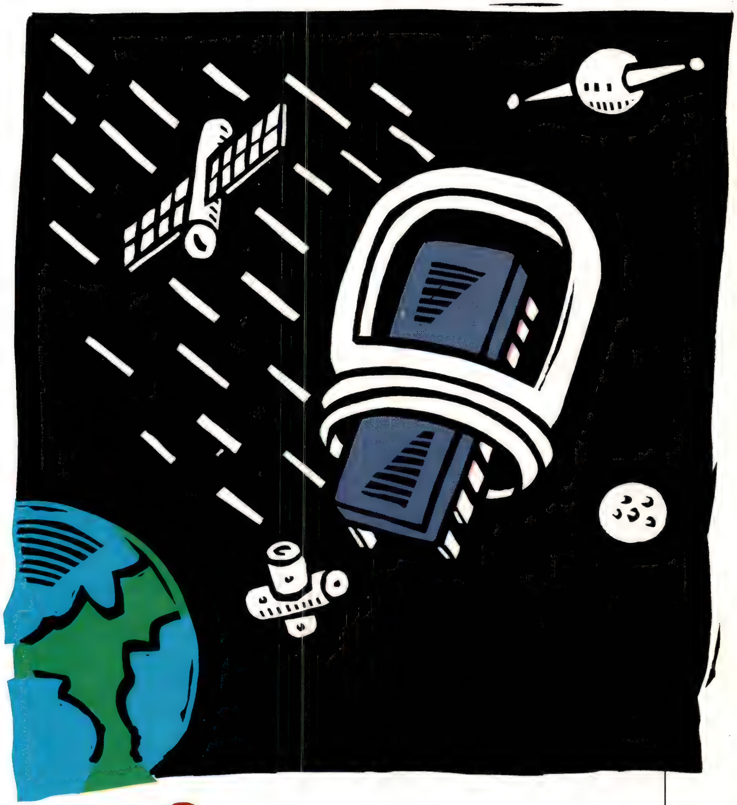
Later, chip developers realized that hardening CMOS further was a matter of insulating individual transistors from one another. They found that by building silicon circuitry on an insulating substrate of synthetic sapphire, or by somehow growing an insulating layer onto the silicon substrate itself, they could produce still harder circuits.

More recently, IBM Corp.'s Federal Systems Division in Manassas, Va., and Honeywell Inc.'s Solid State Electronics Division in Colorado Springs, Colo., have pushed straight CMOS as potential solutions to even the most stringent rad-hard problems. Using extensions of the processes they developed for the Pentagon's Very High Speed Integrated Circuit program, both companies have produced rad-hard CMOS 64-Kbit static random-access memories with SDI funding, using an isolation technique that essentially amounts to building a silicon wall and moat around each transistor. Their success has thrown the rest of the rad-hard world into a tizzy.

Unlike most rad-hard programs, which require only a modicum of memory and which offload most if not all of the processing needs to ground-based systems, SDI satellites must be capable of instantaneously reacting to nuclear events around the globe. And their need to handle tremendous on-board computing tasks means they will require levels of memory capacity never before seen in space-based systems. "SDI birds are memory-hungry," says the Army's Dudney. "Little 4- and 16-Kbit memories aren't going to do it."

Hence the extensive investment in SRAMs in virtually every technology, from GaAs—where 16-Kbit SRAMs are now available—to silicon. Having successfully developed 64-Kbit silicon technology, IBM and Honeywell are now working on the 256-Kbit level. Other funding, from SDI and the DNA, has boosted development of a silicon-on-insulator 64-Kbit SRAM from Texas Instruments Inc. of Dallas and a silicon-on-sapphire 64-Kbit part from General Electric Co.'s Microelectronics Center in Research Triangle Park, N. C.

These new technologies are beginning to edge out the oldest, silicon bipolar, which is currently flying in more satellites than any other. Silicon bipolar was the first technology to reach a high enough maturity level to satisfy the historically cautious space community. But this process is today very limited in den-



Gallium arsenide is tougher than any silicon technology but is plagued by high cost, low yield, and low circuit density. The Pentagon has cut back GaAs funding by more than half

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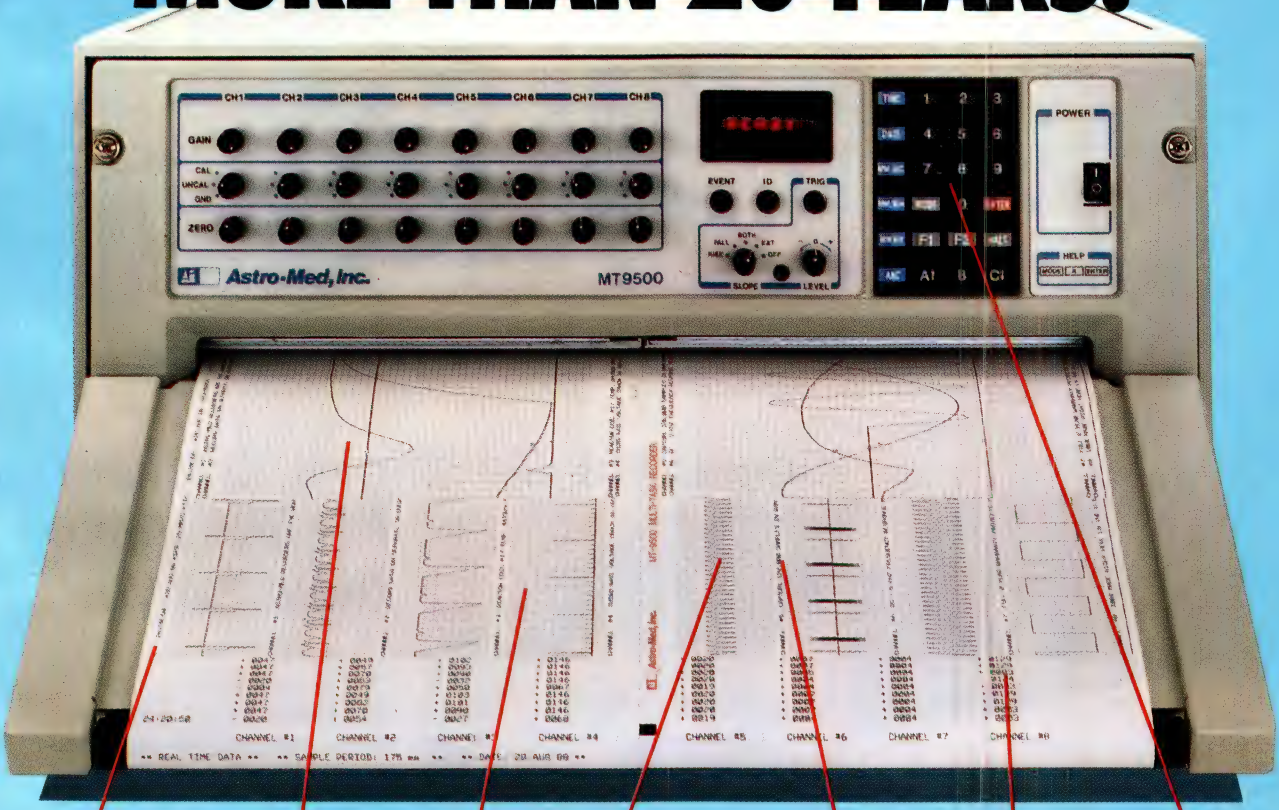

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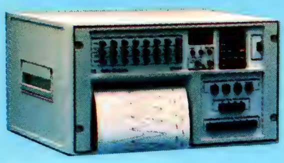

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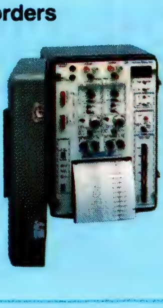

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Circle 12

THE NEXT GREAT HOPE: DIAMOND CHIPS

Silicon in all its varieties dominates today's market for radiation-hardened microcircuits, but scientists say the technology is ultimately too soft for the harshest radiation-packed environments. Their slogan: silicon lasts a while, but diamonds are forever.

Diamonds? Well, diamond semiconductors. If engineers can master the fine art of growing diamond substrates, diamond chips—not the kind that go into earrings, but working electronic circuits etched into diamond substrates—will be the preferred technology for all space and nuclear applications. No matter how advanced silicon or gallium arsenide technologies get, both materials will always be limited by inherent characteristics that, sooner or later, make them vulnerable to radiation damage. Not so diamonds.

"The higher hardness in diamond is going to run circles around everything else," says Dwight Duston, director of innovative science and technology at the Strategic Defense Initiative Organization, which has spent about $13 million in diamond research in the last four years.

Of all potential semiconductor materials, diamond has the highest breakdown voltage, the highest saturated electron velocity, the highest thermal conductivity, and the lowest dielectric constant. "Combine all those things and what you get is high power, high frequency, and rad-hard," says F. Thomas Wooten, vice president for electronics and systems at the Research Triangle Institute in Research Triangle Park, N. C., which has an ongoing diamond program funded in part by SDIO. "Diamond technology is stimulating a lot of interest."

What's more, diamond has mainstream potential in non-rad-hard markets. Any application where high frequency, high speed, and the ability to operate at high temperatures are needed is ripe for a diamond solution, say officials at SDIO, the Office of Naval Research, and several private laboratories that are working on diamond development.

The high-temperature operation is particularly attractive for satellite applications, since 65% of the average satellite is dedicated to thermal management, Duston says. Since diamond circuits could operate at upwards of 600°C—475°C higher than silicon or GaAs—much of that cooling equipment could be eliminated. That would give satellite designers the chance to greatly increase a bird's capability or to decrease its size, so that smaller, less expensive launch vehicles could be used. Immunity to heat would also permit the use of diamond chips inside aircraft engines or nuclear reactors to monitor performance.

But immunity to heat is only one facet of diamond's brilliance. Based on a formula developed in 1972 to derive "figures of merit" for large-scale integrated-circuit materials, diamond is at least 32.2 times superior to silicon, says Max Yoder, a program manager at the Office of Naval Research. Another formula developed for microwave and millimeter-wave ICs rates diamond 8,200 times better than silicon and nearly 1,200 times better than GaAs, the preferred MMIC technology.

"If we could build diamond semiconductors today, we could revolutionize the Mimic program," says Duston, referring to the Pentagon's five-year, $250 million effort to develop high-density MMICs.

And there's the rub: diamond semiconductors can't be built today. One researcher, Michael Geis at the Massachusetts Institute of Technology's Lincoln Labs in Lexington, Mass., has had some success in building circuits on natural diamond. But fabricating dense circuits in volume will remain nothing but a pipe dream until someone learns how to make usable diamond substrates.

Natural diamond is too expensive and stones are too small to be used for anything but research, so synthetic diamond is the key. The problem, says Duston, is that diamond "has a hard lattice constant to match."

So while it can be grown epitaxially with relative ease, finding a suitable substrate to grow it on has so far perplexed scientists. Without a good lattice match, growing anything more than an ultrathin diamond layer is impossible—the material will crack under the strain of the mismatched molecular structures.

There are materials that do match diamond's lattice, says James A. Hutchby, director of RTI's Center for Semiconductor Research. But none of these are capable of withstanding the 700-to-800°C temperatures that diamond must be grown at. The institute's latest hope: finding a copper-nickel alloy that can come close to matching diamond's lattice.

Meanwhile, researchers at Crystallume, a Menlo Park, Calif., company, are taking a different tack. They're trying to develop a lower-temperature process for growing diamond that might allow the use of lithium-fluoride and other materials that, while they match diamond's lattice closely, disintegrate at between 300 and 400°C. If they can grow diamond at a low enough temperature, they can use these substrates to get started and then burn them off at a later stage in the chip-making process, says SDIO's Duston.

Likewise, the Naval Research Laboratories are also interested in lower-temperature processing, says James Butler, an NRL researcher. "Right now, we sort of have a simple-minded view of why diamond can be grown by chemical vapor deposition," he says. "The next aspect of our research is to understand the surface chemistry of diamond so we can grow the material at lower temperatures." *–T. N.*

The key to producing diamond ICs is finding a substrate to match diamond's unusual lattice

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Circle 42

HERE COME THE TEMPS

BY
LARRY
WALLER

HIRE RATE IS SOARING

Electronics-industry managers are relying more heavily on contract engineers and third-party development houses as pressures on profit margins dictate keeping a leaner full-time staff

There's a valued new employee on the scene in the electronics industry these days, but you won't find his or her name on the regular payroll roster. The engineer, designer, or project manager in question is a "temp"—a highly skilled hired gun brought on for a particular project with a limited life span.

Though using temps is not a new concept, the hire rate has soared, spurred by heightened competition that puts a premium on a company's ability to change its work force quickly in response to changing technology. Hard statistics are difficult to come by, but some sources believe high-technology firms account for up to 25% of all salaries paid to temps in the U. S. today. Another index of the robustness of the trend is found in the temp-agency business itself, which has scored annual growth rates of more than 20% over the past 10 years running.

Hand-in-hand with the increasing reliance on outside help—whether individual contractors or those recruited through a high-tech temp agency—is the related phenomenon of third-party development houses. Such businesses, which in effect are subcontractors that handle a project from the design stage through pilot manufacturing, are flourishing. As an industry, they've skyrocketed from a mostly insignificant role a decade ago to be worth a combined $1 billion annually, according to estimates by business consultant Arthur D. Little Inc. of Cambridge, Mass.

A notably open-minded bunch, electronics-industry managers have long been hiring temps to smooth out workload peaks or to fill in for absent hands. As far back as the mid-1970s, they discovered that skillful weaving in of outside talent could give them an edge over the competition. In fact, the peaks and valleys associated with the semiconductor business cycle are tailor-made for temps. Motorola Inc.'s Semiconductor Products Sector, for one, has avoided the heavy layoffs that come with the down part of the cycle by depending more heavily on contract labor than its peers.

But today, competitive pressures on profit margins require keeping the leanest possible full-time staff and make finding quality temps more urgent. Technology talent usually comes through technical service agencies, which supply designers, engineers, and scientists as readily as Kelly Services agencies deliver office help. These "nonstandard types of staffing," as the Conference Board, a business-research organization, calls temps, may be referred to as alternative, contingent, or peripheral employees. Some talk about the trend as a "core-ring" concept, where a work force is divided into a core of full-time workers surrounded by an

THE SALARY IS ONLY THE BEGINNING

Base Salary	$200.00
Mandatory Payroll Taxes	25.20
Time Not Worked (vacation, holidays, sick days, paid breaks from work)	29.60
Hiring and Administrative Costs (training, bookkeeping, miscellaneous clerical work)	14.00
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TOTAL COST	$320.20

SOURCE: UNIFORCE

Decker, is choosing personnel "who truly want to be temporaries." Although salaries are comparable with those of full-time counterparts, the jobs carry no medical, pension, or other benefits, so the ideal hires are retirees, students, or part-timers who have coverage elsewhere. The bedrock requirement is that Force workers cannot use temp jobs as stepping-stones to permanent slots at HP. "This is not a screening device" for full-time employment, Decker says. To this end, there are built-in time limits in two categories: contract workers of from one to six months, extendable to two years maximum; and pool workers who come and go, to a total of 1,400 hours a year. So far, attracting the right mix of workers has been no problem, the company says.

Part of the impetus for Flex Force springs from HP's no-fire policy, a stance that cost it dearly in 1985. During that downturn, HP kept several thousand unneeded workers on its payroll and "learned a lesson," Decker says, about how temp help interleaved with the permanent staff might ease the pangs without violating the no-layoff policy.

PIONEERING EFFORT. With its vast resources, HP can afford to hand-tool an internal temp force to precise needs. "It is one of the programs that is particularly interesting," notes Helen Axel, an economist at the Conference Board. "It is a positive approach that is testing the waters." But most other high-tech firms have to depend on agencies to supply them, creating opportunities these temp outfits are eager to meet. The action is spirited both in specialized technical agencies that are proliferating throughout the country and in general-purpose temp companies that are adding high-tech workers to their employee rosters.

With the added interest has come a change in attitude, says Michael Iandoli, executive vice president of Technical Aid Corp. of Newton Upper Falls, Mass. "Temporary technical talent commands more respect today than 10 years ago," he says. His company, located adjacent to Boston's Route 128 electronics and computer hotbed, is 20 years old this year, and Iandoli can't think of a major company in the region that hasn't used its talent bank. The payroll averages about 9,000 persons per week, he says, from office locations throughout the U. S. in three major areas: design engineers and draftsmen; software personnel for business applications; and software designers and programmers for scientific tasks.

Most executives say that in the minds of their clients, the watershed for temporaries came during the major recession in 1981-82. "That was the jump-off point," says Phil Bratspis, president of United Temporary Personnel Services in Brea, Calif. "Before that, companies primarily wanted work-overload and vacation relief—we were a necessary evil." But the concept of flexible staffing, allowing companies to hold their direct work force to a minimum, then became so attractive that "overnight it changed."

Also contributing was the word- and data-processing revolution brought on by the personal computer, which "parallels the growth of temporary companies," he says. "Most companies buying the equipment couldn't run it, and this forced them to come to the temporary-help industry, which had people who could."

A new twist in the technology field that's giving strong signs of taking off for United involves managing entire production plants for clients on a turnkey basis. The firm now has a half dozen such facilities-management projects, compared with none a year ago, says Bratspis. This approach allows the phased use of temporaries as what amounts to "just-in-time" personnel. Expect to hear more of JIT temps, says Bratspis, because the concept dovetails so smoothly with what may be the hottest idea for increased productivity now being pursued in the U. S.

DESIGNERS. The bulk of agency personnel, however, is employed not for JIT reasons but for design projects, says Jerry Kapalko, senior vice president of temp supplier Olsten Corp. of Westbury, N. Y. "There was a tremendous expansion in this market when companies realized the design side of their business was cyclic, and stopped hiring full-time employees to do what amounted to a part-time job." Even the hefty premiums that clients must pay for a highly skilled temp designer—which could amount to as much as 50% more than a typical salary—is no hindrance: "They know the work will go away in a few weeks or months."

If hiring design specialists on a project basis works well for a growing list of firms, then it makes sense for many to take a further step into turnkey product development by third-party houses. The emergence of Tidewater Associates Inc. during the past several years has shown what these houses have to offer. Founded in 1984, the Union City, Calif., firm has built design expertise in some of the hottest product categories, along with an enviable client list. It offers one-stop development, from concept to pilot manufacturing, or handles any part of that process.

A successful series of assignments helped overcome ingrained industry resistance about letting key research and development move outside direct control, says founder and chief executive Bernard Daines. Besides delivering the goods with the promised performance, he says, Tidewater does it on a stepped-up schedule that clients couldn't hope to match internally. "We have a different mentality, geared to a faster pace," he says. Unlike contract engineers from temp firms, Tidewater does all the work at its own site with the help of the newest computer-aided design gear and a design team "at the cutting edge, which would be prohibitively expensive for most organizations," Daines says.

ASIC SPECIALISTS. It is not coincidental that Tidewater's core technology is in application-specific integrated circuits, which support most new products. All companies are aware of the value of ASIC advances, Daines says, "but haven't bitten that bullet yet" in terms of in-house expertise. That's where Tidewater steps in.

Among the jobs that have propelled Tidewater's revenue to more than $8 million currently was the development of complex printed-circuit boards for a Pacific Bell trial communications system at an unheard-of one-a-week pace for some 35 weeks. When Bell & Howell Co. asked Tidewater to streamline the design for an optical-disk-based system to be used as an on-line graphics data base, the firm responded posthaste. Within five months, it created system architecture, designed hardware and software, and packaged the product for beta testing. Since speed in getting a product to market is preeminent among managers' concerns, says Daines, Tidewater's turnaround time justifies its stiff fees, which can reach six figures. "A substantial share of Tidewater's business stems from repeat clients and referrals," he says.

Additional reporting by Lawrence Curran and Jack Shandle

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Circle 2

FOR LCDs

BY
SAMUEL
WEBER

LCDs are finding their way into a new generation of small-screen TVs for both the consumer and nonconsumer markets, including this one set into an airline seat. The technology is also being primed for the large-screen HDTV arena.

ment and control of equipment, as well as by the use of redundancy in their designs.

As their name implies, LCs are materials with an orderly molecular structure but which have the properties of a liquid. The most common LC material in use today is the so-called nematic, in which the molecules are all oriented in the same direction. A recently developed variation is twisted nematic (TN), in which the LC molecules form a twisted helix.

A display is formed by sandwiching the nematic material between two glass plates. Without an applied voltage, the molecules remain twisted. Light entering the upper polarizing plate becomes oriented in one direction and passes through the twisted LC material, which rotates the polarization by 90°. The light's orientation now matches that of the rear polarizing plate and passes through, yielding a bright display.

With a voltage applied, the LC molecules line up in the same direction perpendicular to the polarized light. This blocks the light, yielding a dark display. To implement a graphic or alphanumeric display in its simplest form, an array of row-select electrodes is formed on one piece of glass and an array of column-data electrodes is formed on a second piece. Voltage applied to these causes the liquid crystal to act as a shutter, either transmitting or blocking light.

The earliest TN liquid-crystal displays suffered from poor contrast and narrow viewing angle, and they degraded at elevated temperatures. Continued improvements in recent years have overcome most of these problems. A further advance was the development of the supertwist (STN) display: with the addition of another LC polarizer plate, it yields improved contrast and viewing angle. But such displays had a characteristic blue tinge that users didn't like. To overcome this, the double supertwist (DSTN) LCD was developed. In the DSTN approach, an extra color-compensating LC glass substrate is added, resulting in an almost pure black and white display with double the contrast of the STN and a better viewing angle. Most black and white LCD panels today use the DSTN technology.

One way to improve the quality of DSTN black and white displays is to increase the twist angle of LC molecules. This creates a steeper distortion vs. voltage curve, resulting in a sharper transition threshold from off to on. When rapidly multiplexed, the result is a high-contrast, wide-viewing-angle display. Most STN displays have an angle of 180° or more. Recently, LCDs with twists of 270°, such as the Hypertwist from Tektronix Inc. of Beaverton, Ore., have been introduced for even higher contrast and greater viewing angle.

But DSTN produces greater light-transmission losses than the STN process, so it needs an intense backlighting source—a requirement that results in increased power consumption, thickness, and weight. Recently, Japan's Hitachi Ltd. and Toshiba Corp. introduced DSTN displays that replace the extra layer of LCD glass with a thin polymer film. Both companies claim substantial reductions in weight, thickness, and power consumption.

Because of the limitations of the STN and DSTN approaches, LCD developers are today embracing active-matrix technology to get the response time and resolution required of a high-quality color display. Here, a nonlinear element such as a diode or transistor is placed in series with each LC element, with a resultant in-

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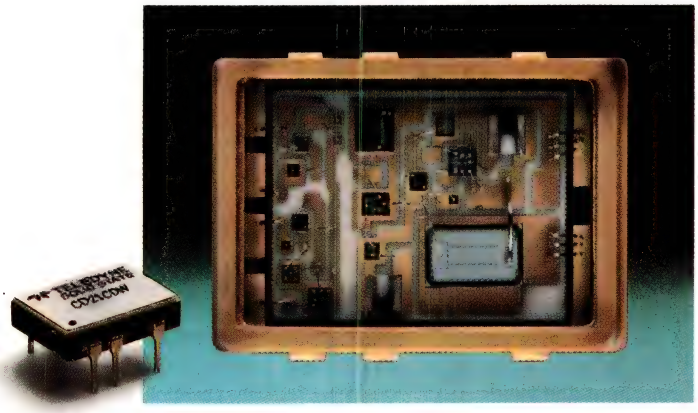

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ELECTRICAL CHARACTERISTICS
(−55°C to +105°C unless otherwise noted)

	Min	Max	Units	
Bias Voltage (V_{BIAS})	3.8	6.0	V_{DC}	See Note 1
Bias Current (I_{BIAS})		15.0	mA	$V_{BIAS} = 5 V_{DC}$
Control Voltage (V_{IN})	0	18.0	V_{DC}	
Control Current (I_{IN})		250	µA	$V_{IN} = 5 V_{DC}$
Turn-Off Voltage $V_{IN\,(OFF)}$	3.2		V_{DC}	
Turn-On Voltage $V_{IN\,(ON)}$		0.3	V_{DC}	
Continuous Load Current I_{LOAD}		1.2	A	−55°C to +25°C
		0.7	A	+85°C
Output Trip Current (I_{TRIP})	2.4 (Typ.)		A	+25°C, 100ms
On-Resistance (R_{ON})		0.65	Ohms	
Turn-On Time (T_{ON})		1.5	ms	
Turn-Off Time (T_{OFF})		0.25	ms	
Status Voltage (V_{STATUS})	1	18	V_{DC}	
Status Current (I_{STATUS})		2	mA	$V_{SAT} \leq 0.3 V_{DC}$ See Note 2

Notes:
1. Series resistor is required for bias voltages above $6V_{DC}$. $RS = (V_{BIAS} - 6\,V_{DC})/15$ mA
2. A pull up resistor is required for the status output. $R_{STATUS} = (V_{STATUS} - 0.3)/I_{STATUS}$
3. Output will drive loads connected to either terminal (sink or source).
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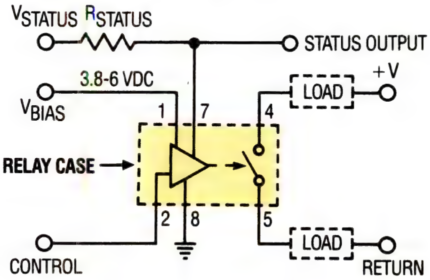

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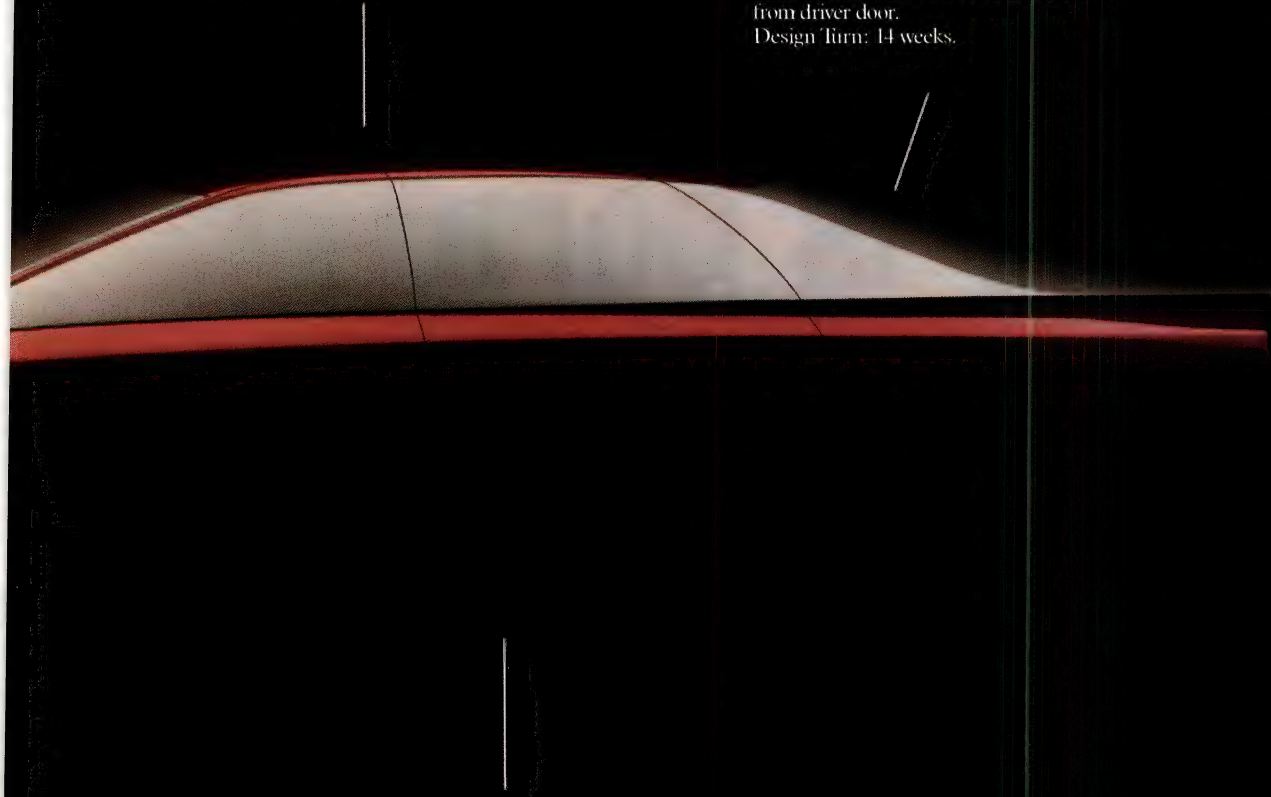

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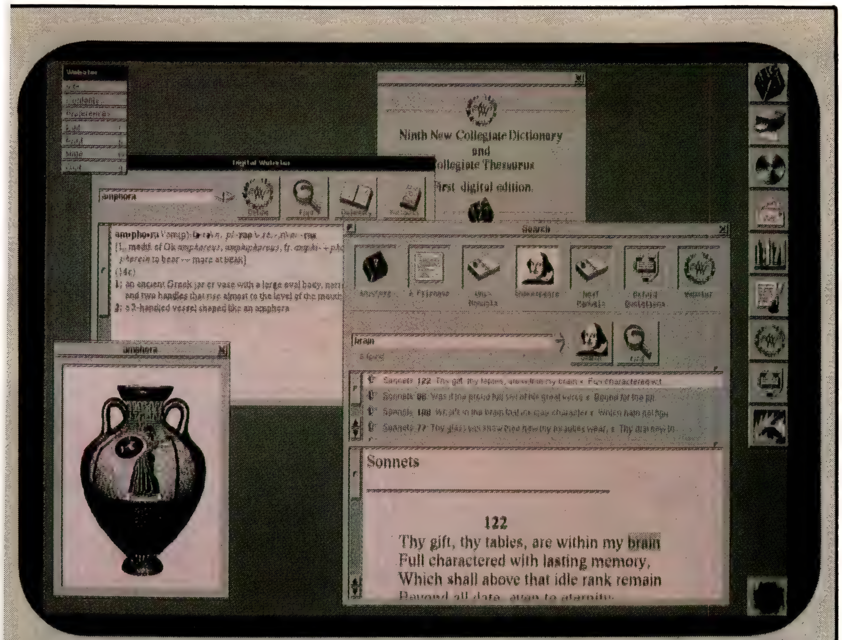
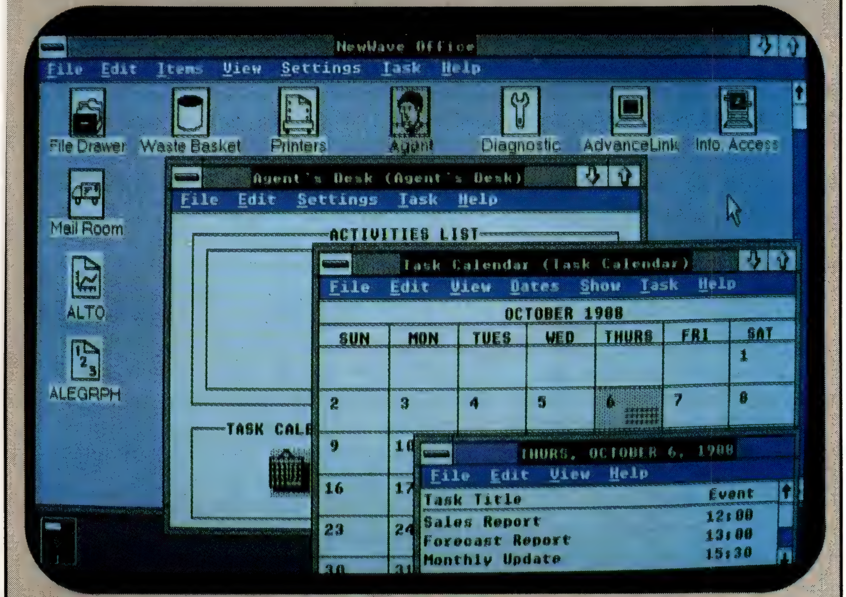


am·pho·ra \'am(p)-fə-rə\ n, pl -rae \-,rē, -,rī\ or -ras
[L, modif. of Gk amphoreus, amphiphoreus, fr. amphi- + phorein to bear — more at BEAR]
(14c)
1: an ancient Greek jar or vase with a large oval body, narrow cylindrical neck, and two handles that rise almost to the level of the mouth
2: a 2-handled vessel shaped like an amphora

Sonnets

122

Thy gift, thy tables, are within my brain
Full charactered with lasting memory,
Which shall above that idle rank remain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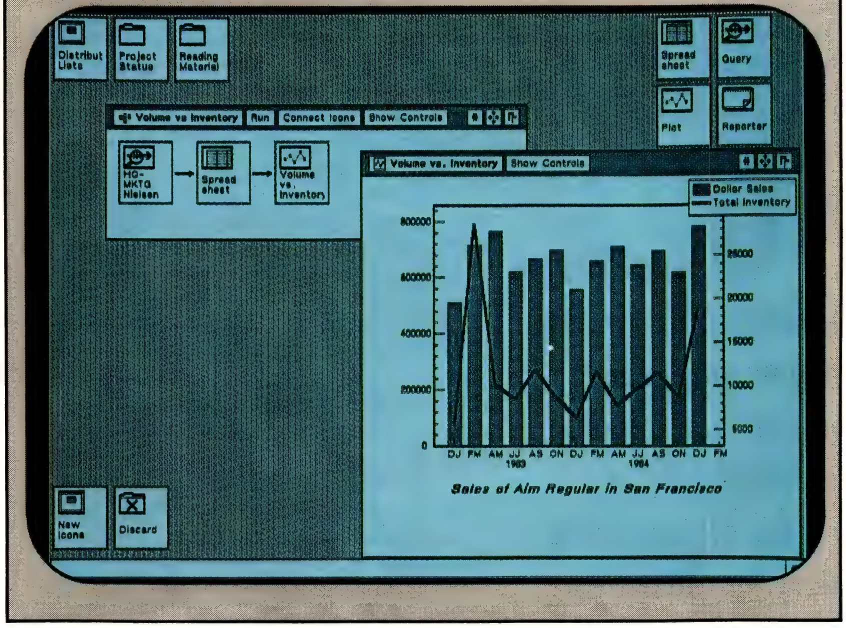

For the end user, object-oriented programming results in an easy-to-use interface laced with windows, icons, and pull-down menus. From top, the Next interface (the Shakespeare icon calls up the complete works), Hewlett-Packard's NewWave, and Metaphor's Data Interpretation System. Programming in these environments is a matter of simply manipulating objects.

mous structure, often referred to as an object. This concept is called encapsulation. "A system that embodies the concept of data structures and methods being stored together has an object model," says Liddle. Another important concept is reusability. Because objects are self-contained, they can serve as standard software modules to be used over and over in a variety of programs.

Finally, "to be truly object-oriented, a system must also embrace the notion of classes and inheritance," says Liddle. Objects are placed in an inheritance hierarchy and new objects can be created simply by defining how they differ from their parents. New objects inherit the characteristics (data structure and procedures) of all preceding objects in the hierarchy.

A STRETCH. In some systems, multiple inheritance allows subclasses to inherit characteristics from more than one branch of the hierarchy. Object generation becomes simpler and simpler as the hierarchy grows. This concept is often called extensibility. One of the big advantages of object orientation is that the more subclasses that exist, the more code can be reused. A disadvantage is that as subclasses are added, programs get bigger and lots of memory is required.

These ideas spring from "three independent and separate evolutions of object-oriented technology," says Daniel Wood, manager of software-product planning at BiiN in Hillsboro, Ore. First, he says, is the graphics world, with its windowing and iconic interfaces, such as those used in Apple Computer Inc.'s Macintosh and in such software as X Windows and Microsoft Windows. Second is conventional programming, where in the face of the inadequacies of structured programming designers have hit upon an object-oriented concept, defining subunit building blocks for creating complex systems. In Ada, for example, the definition of objects is not all that different from the object definition in the graphics-object world.

Third is the world of computer-system architecture exemplified by BiiN, Next, and the IBM AS/400. Object-oriented technology offers a new way to think about computing—a human-centered way. Its critical theme is based on the observation that the things (objects) that we wish to model in computing change much less rapidly than the ways we wish to use them. Object-oriented technology offers a way to describe the content and behavior of application entities (objects) in an efficient, controlled, and manageable way. Once objects are defined, they can be freely used without worrying that their behavior will change as the behavior of other objects changes. For example, a change in the detailed behavior of an account will not cause changes in the definition of a ledger.

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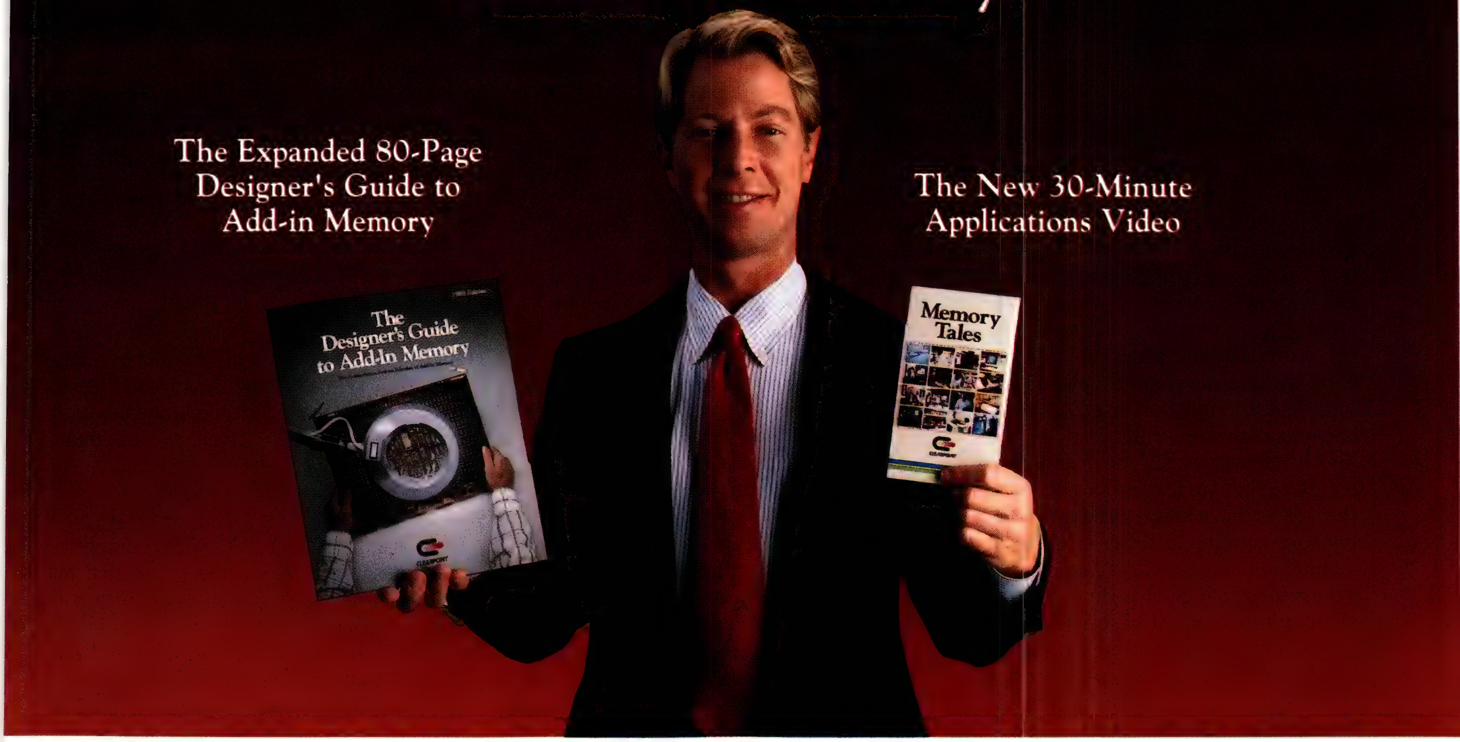
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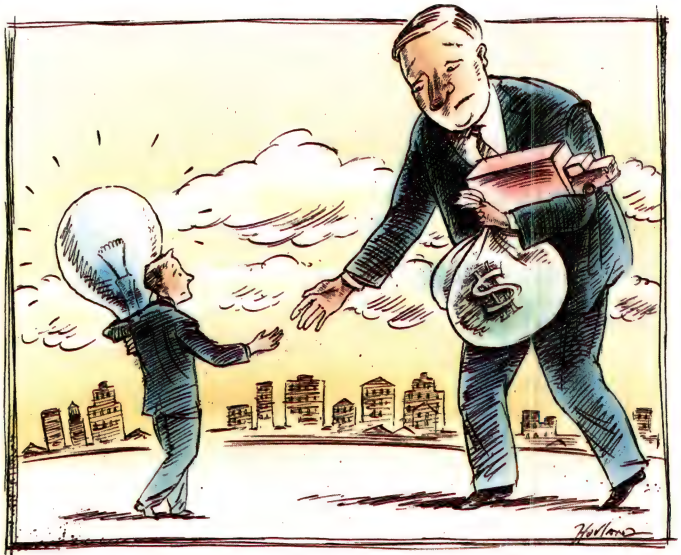
*Christopher Kreager, Systems Specialist, UNITED DATA SYSTEMS

Circle 2

BY JACK SHANDLE

UNITED WE CONNECT

A rash of new partnerships in LANs and WANs is raising hopes that true standards-based multivendor networking may be on the way. The big winner is the customer



Desktop-to-desktop connectivity isn't just a pipe dream anymore. Partnerships and acquisitions among local-area and wide-area networking companies are putting real muscle behind the long-heard call for standards-based, multivendor networking. Simply put, companies smaller than Digital Equipment Corp. and IBM Corp. just can't go it alone in the wide, wide world of global connectivity. "We all have the same strategic plan: to offer complete networking solutions for our customers," says Pradman Kaul, president of Hughes Network Systems in Germantown, Md., one of the world's premier WAN companies.

A number of firms, including Hughes, are teaming up to fill gaps in their corporate offerings. Each deal is unique, but most share three themes. First, TCP/IP—the Transmission Control Protocol/Internet Protocol—is the de facto interoperability standard. Anybody without TCP/IP capability across the board had better get it. Second, network management is the Achilles heel of connectivity. Building in a coherent, powerful, and efficient set of network-management functions requires top-to-bottom cooperation between LAN and WAN vendors. Third, global networks need global sales and service support.

In a recent announcement, Hughes revealed plans to acquire Sytek Inc. of Mountain View, Calif., a leader in large broadband LAN installations. The acquisition follows on the heels of Hewlett-Packard Co.'s teaming with LAN-vendor 3Com Corp. of Santa Clara, Calif., in a sales and marketing partnership. HP runs one of the largest in-house WANs and is aggressively marketing its WAN expertise and products.

Not to be outdone by rival 3Com, the Provo, Utah-based Novell Inc. on March 23 announced a merger with Excelan Inc., a LAN protocol specialist based in San Jose, Calif. Earlier in the year, Excelan forged a marketing partnership with mainframe-to-mainframe networking wizard Network Systems Corp. of Minneapolis, which itself has just unveiled another marketing agreement, this one with Wellfleet, a WAN vendor based in Bedford, Mass.

Although networking companies are universally committed to supporting standards, the partnership trend makes it clear that true standards-based, multivendor connectivity is still in the future. Increasingly, corporate customers have migrated to private WANs to connect their LANs, says Mike Sprayberry, director of integrated network solutions for CAP International, the Norwell, Mass., analysts. But LANs "grew out of the backplane of personal computers and work stations," he says, while WANs were conceived as data bridges between mainframes. This makes interconnecting LANs over a WAN tough.

"In one instance, we found a company that had 13 different network-management systems to deal with when it started to internetwork its LANs," says Bill Way, Network Systems' product-line manager. The solution being sold by the bevy of new partnerships is essentially one-stop shopping at a multivendor store, with service contracts and guarantees that everything will play together. "In these strate-

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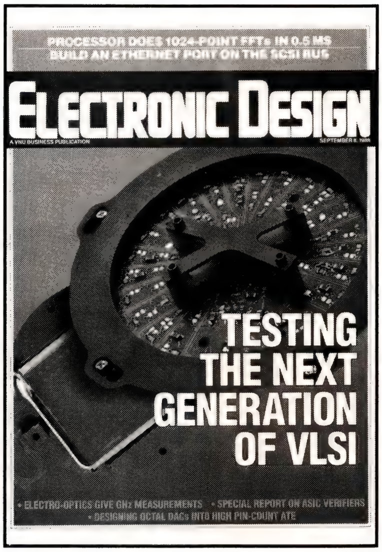
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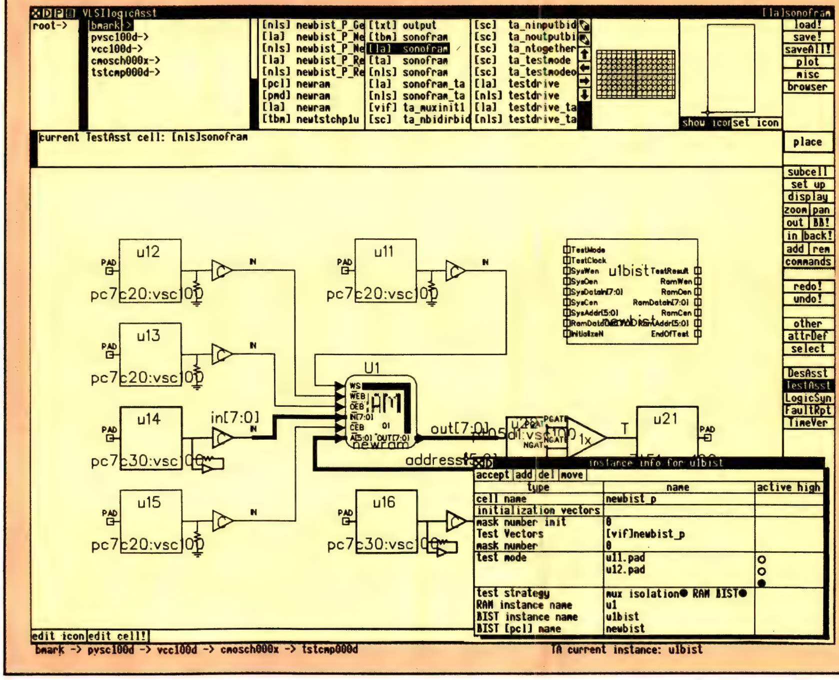

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initialization vectors		
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test mode	u11.pad u12.pad	○ ○ ●
test strategy RAM instance name BIST instance name BIST [pcl] name	mux isolation● RAM BIST● u1 u1bist newbist	

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TA current instance: u1bist

In testing a hypothetical "megochip," the tool can add a built-in self-test (BIST) block upon the designer's command; to do so, the user simply fills out a three-line menu.

three different forms. There are large blocks, such as the microprocessor cores found in a foundry's ASIC library; compiled cells, such as random-access and read-only memories, and programmable logic arrays; and semicustom blocks containing logic the designer has created with standard cells.

For the large microprocessor-type library cells, VLSI Technology provides a comprehensive set of test vectors for 95% fault coverage. The silicon compiler that produces a ROM, RAM, or PLA produces all the test vectors needed to provide this same level of fault coverage for those blocks. Lewis says that if a designer builds an ASIC with just these two types of big blocks, Test Assistant's wiring and testing procedure will be fully automatic and fault coverage of 95% or higher will be assured. However, for a semicustom block made up of standard cells, the designer does have to perform some test-program development.

To use the tool, the designer first gives the Test Assistant the netlist of the ASIC for which a test program is to be developed. From a block-level representation of the design, he selects the first block to be isolated, and the tool shows how it will route the block's I/O pins to the ASIC.

In the isolation phase, the tool installs multiplexers at the block's I/O pins to switch them out of the normal signal-flow path and route them to the ASIC's I/O pads. A rule that the tool adheres to is not to insert more than one level of multiplexer between the block's I/O pin and its internal circuit. This ensures that the test circuits do not affect the timing in the ASIC's critical paths.

INTERACTION. At any point in the tool's operation, the designer can interact with Test Assistant to change the implementation manually. For example, the operator can direct the tool not to multiplex certain ASIC I/O pads that lie in a critical path. If this restriction means there will not be enough I/O pads to access the I/O pins of internal blocks, Test Assistant can change any pad specified as output-only into a bidirectional pad to attain the additional number required.

If the designer accepts the tool's proposed isolation and signal routing, Test Assistant automatically changes the netlist to incorporate the test circuits.

Thereafter the process is repeated with all the other blocks. Besides isolating and wiring, the tool also creates the control circuit needed to configure the ASIC in test mode and to switch each individual block to the I/O pads for testing. It adds this circuit into free space on the ASIC and routes the test-signal wiring between the control unit and each block.

To activate the test circuit, the designer can specify a vector that, when applied to the ASIC's I/O pads, switches the test circuit on. Using a vector eliminates the need to use an I/O pad to switch the test circuit on and off. With the test circuit turned on, each block can be individually switched. At the I/O pads, a component test system can send stimulus into and measure responses from the block.

To create test programs for a semicustom block, the designer typically produces test vectors using simulation vectors developed in the design phase along with vectors written later to increase fault coverage. He also performs a fault simulation to determine if the desired fault coverage has been achieved. Once the test program is developed, Test Assistant isolates and reroutes the semicustom block's I/O pins to the ASIC in the same way it handled the other blocks.

One important function of Test Assistant is its built-in self-test (BIST) capability. The designer can direct the tool to add a linear feedback shift register to the input and output of a compiled block. At the input, the circuit serves as an autonomous pseudo-random pattern generator, while at the output, it acts as a signature analyzer. This is particularly attractive for highly regular compiled RAM and ROM blocks.

"Built-in self-test puts a tester on the chip," Hutcheson says. "It facilitates the device tester's job during production, thus cutting test time." It also facilitates field service, he says, "since the service technician has instruments on-chip to help diagnose a field failure."

In the compiled RAM or ROM block, the compiler can add the signal generator and signature analyzer so that the resulting BIST produces a 1-bit pass or fail indication to one of the ASIC's output pins. Alternatively, the designer can route the block's output pins to the ASIC's I/O pins for analysis by the device tester.

Self-test can also be used on a semicustom block. Here, the designer adds the signal generator and then simulates the operation of the circuit with the pattern generator installed to determine if all the nodes in the design are being tested and if the pattern actually catches each possible fault node.

Because the generator produces the same sequence of random patterns each time it runs, using the linear feedback shift register, the designer can create a circuit that performs an X-NOR logic operation on the responses received from the block. The result is a signature that indicates the block is good or bad. The entire signature can be sent to the ASIC I/O pads for verification.

In the future, the Test Assistant will be able to add level-sensitive scan design to blocks within a chip as an alternative to isolation, VLSI Technology says. Instead of bringing signals to the ASIC I/O pads, it will serially shift test vectors to hidden nodes within the ASIC, stimulate the hard-to-access circuit behind the hidden node, and serially shift the results back to the ASIC I/O pads.

With this powerful tool to drastically cut the time needed to write an exhaustive test program, designers can get back to spending most of their time designing chips rather than worrying about how to test them. ☐

TROUBLE IS BREWING OVER CFCs IN CALIFORNIA

The AEA calls one proposal a potential 'disaster'

by Larry Waller

To John Masterman, it seems only natural that the state of California emerge as a proving ground for legislative efforts to curtail the use of ozone-destroying chlorofluorocarbons. "California continues to be the birthplace of [environmental] laws," observes Masterman, chairman of the American Electronics Association's California Environmental-Occupational Hazards (EOH) Legislative Committee.

Any laws enacted by California concerning CFC use are likely to have a tremendous impact on the U. S. electronics industry, which uses CFCs in the manufacture of a wide range of products [*Electronics,* April 1989, p. 92]. The California state senate is pondering a proposal to rein in CFC use even more severely than has been called for by international guidelines. The proposal pretty well reflects the regulatory mood in the Golden State and perhaps offers electronics manufacturers everywhere a picture of the difficulties and bureaucratic confusion that the future holds for them.

The action in California also illustrates the problems that a trade organization like the AEA faces when it gets a late start in its lobbying efforts. Masterman concedes that the AEA is getting into the environmental hazards game on the state level relatively late. Although the AEA tracks environmental affairs from its Washington headquarters, the scene in California is a hyperactive arena in which the big organization has not played a part for nearly five years.

The AEA is alarmed by the California CFC initiative. If the measure passes in its present form, California's Air Resources Board essentially would gain the power to manage every application for which CFCs could be used. It could determine whether substitutes exist and then mandate their use. The degree of control and the opportunity for error appall Masterman. "It's a bad law that could be a disaster," he says.

Masterman's committee is now working to avert that disaster. It has already had an impact on getting some proposed environmental bills apart from the CFC arena changed before they became state law. One of these would have banned any use of arsine and phosphine gases—both widely employed in electronics manufacturing—within 25 miles of any residence. In its original form, the proposal "would have wiped out the electronics industry," Masterman asserts. Partly through the AEA's efforts, the proposal was changed to bar only the manufacture of arsine and phosphine gases, not their use.

In Masterman's view, the proposed Toxic Gas Model Ordinance for Santa Clara County (Silicon Valley) is a model for how environmental legislation should be approached. The proposal, the product of three major groups that sat down and hammered out an approach acceptable to all, offers a method of assessing the hazard of every toxic gas and providing safeguards for each of them.

Meanwhile, the AEA last November launched a big effort to get what it deems both a balanced outlook and solid technical data to legislators on a continuous basis. Masterman, who is director of health, safety, and environmental affairs for Intel Corp. in Folsom, Calif., notes that the AEA's move into the EOH game from an inactive status requires diplomacy and a deliberate pace, due to the emotionally charged nature of the subject.

The AEA legislative committee, with some 20 companies currently taking part, meets monthly at different locations throughout the state. Plans are afoot to raise funds for a full-time lobbyist in the state capital at Sacramento to monitor legislative doings.

Masterman's committee is likely to have a wider role in the CFC battle than individual AEA member companies in California. Since they lack any other central clearinghouse or sounding board for their environmental interests, companies by themselves are hard put to deal with escalating regulatory and reporting requirements from all levels of government.

Their greatest headache lies in the staggering number of requirements—many of them overlapping—to be met and the range of official bodies overseeing them. A company typically has to deal with about 10 entities, from the federal Environmental Protection Agency through state and regional regulatory groups, right on down to local fire and safety departments and sewer and water districts.

Companies say their chief need is getting up-to-date information about new requirements and how to handle them. "There is no magic wand to bring you into easy compliance with these ever-shifting regulations," says Edwin K. Isely, manager of the Los Angeles office of A. T. Kearney Inc., management consultants with an extensive environmental consulting practice. Instead, companies have to seek these answers for themselves.

Isely and Masterman both advise executives in California to get involved with state and local organizations that are up to speed on environmental issues, particularly the California Manufacturing Association and chambers of commerce. "Stay in touch with your local organizations," says Masterman. "You can't monitor [the issues] by yourself. It's a noble goal, but no one can afford it." ☐

COMPANIES TO WATCH

A JAPANESE GAMBLE PAYS OFF FOR TEST-GEAR VENDOR TERADYNE

The firm regains its Far East foothold with a next-generation memory tester

AGOURA HILLS, CALIF.

Three years ago, Teradyne Inc. took its biggest gamble. Not only did the company decide to sell a next-generation megabit-memory tester into a depressed chip-equipment business, tough enough by itself, but it took on a task that was even more daunting—regaining the foothold in Japan it had lost to stiff competition.

Teradyne's testers are big-ticket items that can carry price tags in the neighborhood of $700,000. And because gestation and sales times are long, it may take years before the company knows how its product is playing in the marketplace.

Now it appears that the Teradyne gamble has paid off. Orders have come in for more than 150 of the new J937 Memory Test Systems, and the smiles at the Semiconductor Test Division in Agoura Hills and at corporate headquarters in Boston are getting wider. Six big Japanese chip makers, whose size and reach set the worldwide standards for dynamic random-access memories, have already taken delivery of 34 units. Leading Korean suppliers with big testing needs have also ordered the systems.

The main reason for the momentum in Japan is the same simple one that underpins all high-tech success stories, says James A. Prestridge, who runs Teradyne's Components Test Group: "The machine is more advanced than what [prospective customers] can get in their local markets." Proving a memory tester with top Japanese firms gives the product an extra boost elsewhere, too, says Prestridge, because the market in Japan is a particularly competitive one.

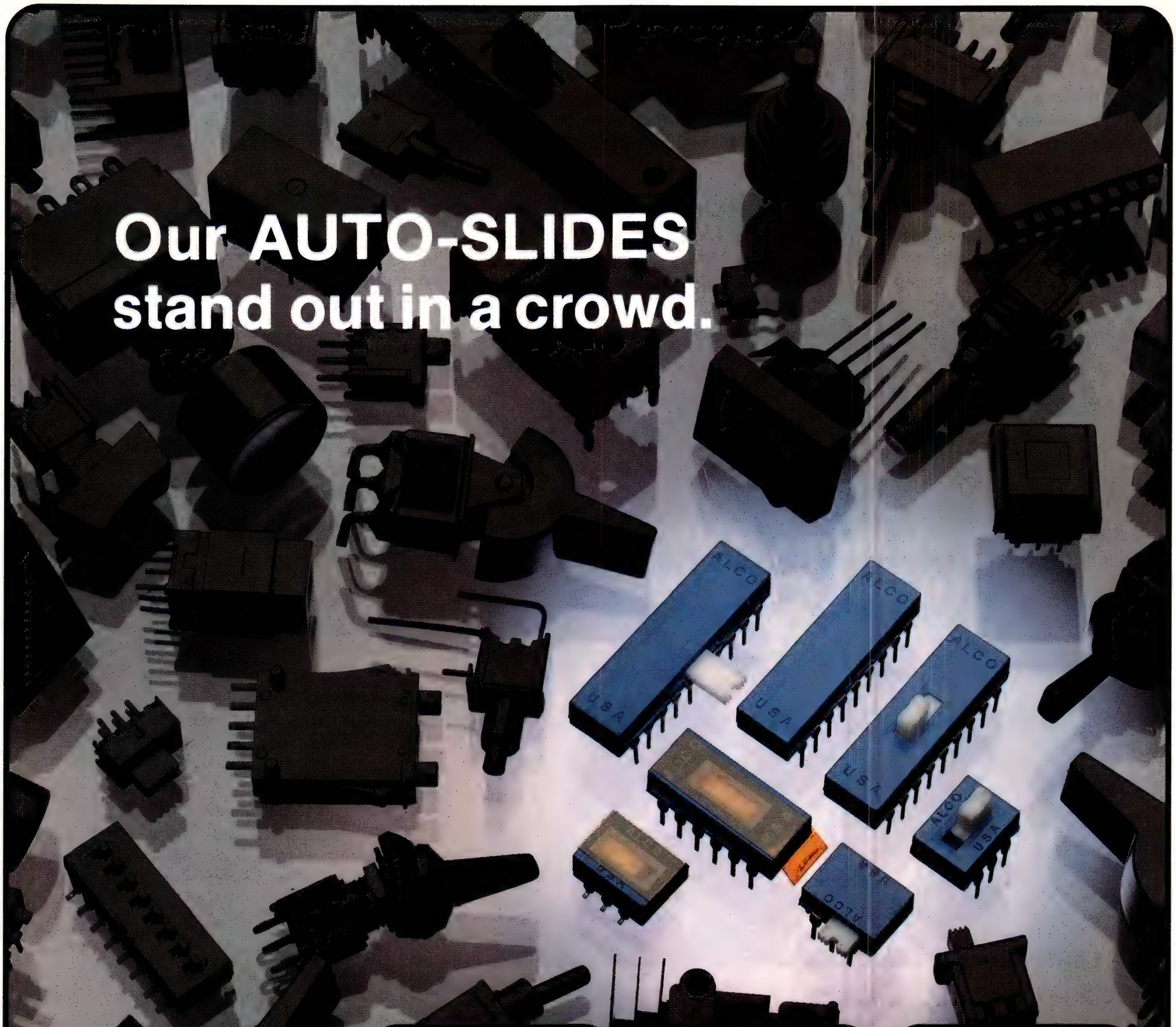
Alex d'Arbeloff, Teradyne's president and chief executive, holds a similar view. "My personal opinion was that we'd be successful in Japan, because we could offer higher performance with better technology," he says. Unlike other sales arms that come under division heads, the operation there reports directly to d'Arbeloff, "because Japan is so important in the semiconductor industry."

Among those admiring Teradyne's Japanese feat is VLSI Research Inc.'s G. Dan Hutcheson, who follows the worldwide tester business. "It was an intelligent decision," he says. "Teradyne had significant technology advantages, and they really went after the market by designing a machine for it." Along the way, "they clobbered the U. S. competition, too."

Teradyne in fact intended the J937 to leave competitors in the dust by pushing tester speed up to a 100-MHz clock and address rate, with accuracies of less than 1 ns. Competing units cannot approach these specifications [*Electronics,* March 31, 1986, p. 45]. Megabit versions of DRAMs need this kind of performance.

Teradyne's strategy was first to sign up U. S. heavyweights IBM Corp. and AT&T Co., then build on the strength of those relationships. Its timing also proved fortuitous because of the 1986 upswing in memory demand, just at the time first installations were taking place. As a result, demand for testers took off faster than even Teradyne expected. Also, Prestridge points out that the six-

Teradyne's J937 Memory Test System has gained ground for the company in Japan. Six big chip makers there have taken delivery of 34 units, which are used for testing dynamic RAMs.



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PEOPLE TO WATCH

AT&T'S KOELTL SAVORS THE CHALLENGE OF TAKING ON MERCHANT CHIP GIANTS

His strategy is based on partnerships with customers, alliances with rivals

BERKELEY HEIGHTS, N. J.

As a young engineer fresh out of New York's Manhattan College and looking for adventure, Dick Koeltl had an important decision to make: would he specialize in locomotives or semiconductors?

Semiconductors—the technology was called "solid-state" back in 1964—won the battle. Koeltl's 25-year odyssey through power integrated circuits, analog-to-digital converters, telecommunications chips, and linear ICs in companies as legendary in the chip business as Advanced Micro Devices, General Electric, Fairchild, and Raytheon was a near-perfect training ground for his new job as AT&T Microelectronics' marketing czar.

"There is all this technological capability here, and for a marketeer, that has to be an exciting prospect," Koeltl says. "Despite its technology, up until now AT&T Co. has not been known for strong marketing."

From a modern, spacious office overlooking the rolling green hills of rural central New Jersey in Berkeley Heights, Koeltl is not that far removed geographically from his cadet days in General Electric Co.'s engineer-in-training program in Schenectady, N. Y. "When I came on with GE," he says, "they had five separate businesses—everything from locomotives to semiconductors. When I got to the semiconductor division, the people all around me were in their 20s. It was obviously a dynamic, growing business."

Infusing more dynamism and growth into AT&T Microelectronics has been at the top of Koeltl's docket since he arrived six months ago to become marketing vice president, fresh from a similar job at GE Intersil. AT&T Microelectronics sells 25% of its ICs in external sales; the rest go to AT&T's various systems divisions.

AT&T's aim is to do more than $1 billion in external sales by 1992, and that means over 50% of its business will be in the merchant market, says Koeltl. If it happens, AT&T Microelectronics would be playing in the major leagues with the likes of Fujitsu, Intel, National, NEC, and Texas Instruments.

The strategy is to get AT&T Microelectronics out of the marketing closet by becoming partners—with customers, and via strategic marketing alliances with competitors. Such partnerships with system-house customers aren't new. Companies like IBM Corp. and Intel Corp. have been pretty successful at it, with Intel producing microprocessors for IBM's personal computers and Personal System/2.

"We're looking at specific markets for equipment segments that fit well with our technologies," say Koeltl. AT&T is "well into" talks with "two or three" major system houses and will be unfurling the agreements as early as the next six to twelve months. Although Koeltl is coy about naming the prospective corporate brides-to-be, he describes them as being in the data-processing, telecommunications, and military markets. "We're looking for major potential markets where we can codevelop technology," he says. One recent example: high-definition TV and Zenith Electronics Corp.

On the competitors' side, AT&T Microelectronics has already teamed up with Intel to exchange technology in areas where product lines are complementary. The agreement is complex, but it boils down to Intel contributing local-area-networking chips and AT&T pitching in its expertise in integrated services digital network chips.

Another prime growth area for AT&T is in better utilization of its silicon foundry capacity. AT&T and Logic Devices Inc. have signed a foundry agreement committing Logic Devices to purchase up to $75 million worth of finished silicon wafers over the next three years.

Aggressively second-sourcing standard parts is also in the cards, "and you'll see results in that arena over the next few months," says Koeltl. "We've got plenty of opportunities to fill out our standard-parts offering." Lastly, price reductions—once seldom heard words in Berkeley Heights—will liven up the company's marketing blitz. AT&T has already slashed the price of its high-performance digital signal processor, the DSP32, by almost 50% thanks to a new plastic-packaged version.

Obviously enjoying the prospect of butting heads with the giant merchant chip makers on three continents, Koeltl talks with exuberance. His selection as head of marketing was atypical for AT&T, which usually promotes from within. "To do

Dick Koeltl's goal is to continue to double AT&T Microelectronics' sales in the merchant market, now at $200 million, each year.

big optics and electronics producer, as a case in point. Of course, government planning will remain a bedrock element of East Germany's economic policy. But the bureaucratic strings are being loosened, giving the combines more leeway to run largely on their own and strive for what East German officials call financial gains—"profits" is still too capitalistic a word for most officials.

In some ways, the efforts of Apitz and like-minded colleagues resemble a form of East German economic *perestroika*—although that term was seldom heard from industry officials at this spring's Leipzig Fair, where VEB Kombinat Nachrichtenelektronik displayed its wares. East Germans prefer to describe the changes as *wirtschaftliche Rechnungsführung*, which, roughly translated, means an economic accounting of balances. Among other things, this concept permits a combine to invest part of its financial gains in its own operations.

GLOBAL NEEDS. Apitz doesn't think the combine's heavy exports to countries in Eastern Europe and the Third World, which are less demanding technologically, will keep it from making high-quality products that satisfy global needs. "The existing concept [for exports] calls for cooperation on a Comecon-wide scale," Apitz says. (Comecon—the Council for Mutual Economic Assistance—is Eastern Europe's equivalent of Western Europe's Common Market.)

Jürgen Apitz is determined to market his combine's telecom technology in the West.

"But we want to increase sales in Western countries, so we must increase capacity and develop a technological base to meet global requirements." In the face of international competition, Apitz adds, "we are forced to stay on a par with other industrialized countries to advance our society, help meet the needs of our home market, and maintain a high export rate."

Apitz is counting on a series of cooperative efforts to help boost his combine's status in the West. The combine has struck a deal with Intracom in Greece involving exchange and transmission equipment. A similar deal is being discussed with Telindus, a Belgian communications equipment maker. And preliminary talks concerning joint projects in other countries have been held with Siemens AG of Munich.

Apitz is the prototypical production man—amiable but forceful and quick of mind. He was trained as a tool and die maker, studied general engineering at the Technical University in Karl-Marx-Stadt, and then worked as a technologist in the plastics industry. Ten years ago he moved into electronics and worked for most of the time as production manager in an instruments factory before being put in charge of VEB Kombinat Nachrichtenelektronik.

The technological challenge Apitz faces is to move his combine from the analog to the digital era and into the age of integrated services digital networks. One of the first results of this effort is the NZ400D, a private-branch exchange for speech, data, and text that features ISDN characteristics. The combine displayed the product at the Leipzig Fair. If Apitz successfully administers the transition to ISDN and turns his organization into an efficient and profitable unit, he will indeed be a true revolutionary in East German electronics. *–John Gosch*

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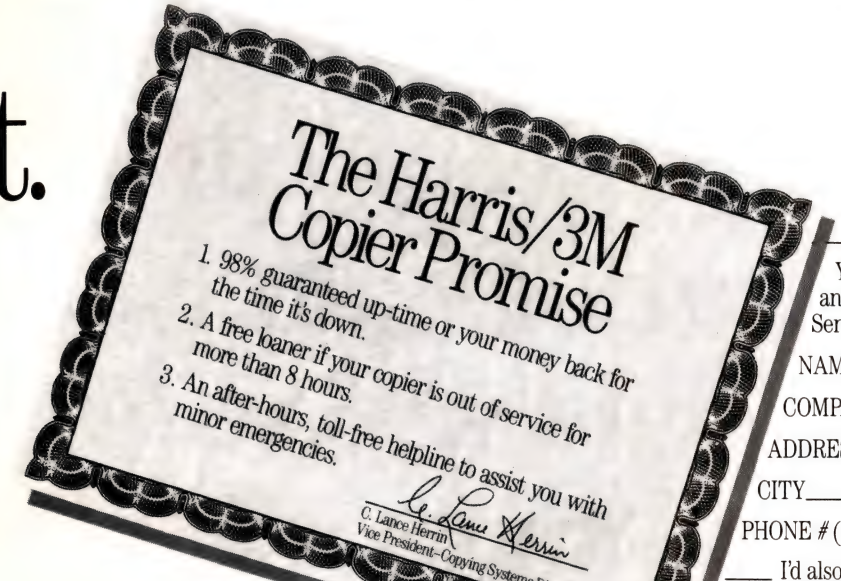
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SKATES: PUTTING DATA GENERAL BACK ON TRACK

WESTBORO, MASS.

The title is a new one for Data General Corp.—executive vice president and chief operating officer. And it's a new one for the man who carries it, Ronald L. Skates. Though he has worked for the big computer maker for less than three years, he is already settling into his role as the right-hand man to the founder, Edson de Castro. Most other senior managers report to him in his new position.

Skates, who took on responsibility for day-to-day operations after giving up his post as senior vice president for finance and administration, in turn reports directly to de Castro. "It's almost a classic U. S. business organization," Skates says. "I'm his only direct reporter, but he's the boss." He adds that the restructuring may be two to three years overdue, "but it didn't happen earlier because the company was on a roll. Few organizations make such changes when they're growing 40% a year."

But after the roll came the rock. Beginning in 1986, Data General's growth slowed, and the company suffered three losing years in a row. It also sustained a $19.5 million loss in the first quarter of this year. But this losing streak may be coming to an end. Significantly, Skates has taken over de Castro's traditional role of explaining financial results. Both say the firm should return to profitability in fiscal 1989, ending in October.

OPTIMISM. Some of the optimism in Westboro these days results from a revamped strategic plan that has three major thrusts: continuing to upgrade the proprietary MV/Eclipse computer line; launching a major initiative in open systems, especially reduced-instruction-set Unix platforms; and making a move into telecommunications and networking.

The first evidence of the telecom initiative was a contract late in 1987 with Japan's NTT Corp. calling for Data General to deliver hardware and software for NTT's private data networks. And Data General unveiled its first RISC work stations in late February.

Skates, a certified public accountant, says he's had a long-standing relationship with Data General from his days at New York-based Price Waterhouse, where Data General was a client. He spent 20 years at the accounting firm and became a partner. "I always liked Data General in those days, and I became familiar with computers and computer companies from auditing them." But he wasn't content to remain strictly a bean counter at Data General. "I've always wanted to be operations-oriented," he says.

Part of Skates's aim at Data General is to "bring a stronger sales and marketing focus to the company. The knock on us is that we have great products but don't seem to be able to sell them well. The focus has been on technology and building a better product so people will beat a path to our door—but that doesn't work anymore," he says. *–Lawrence Curran*

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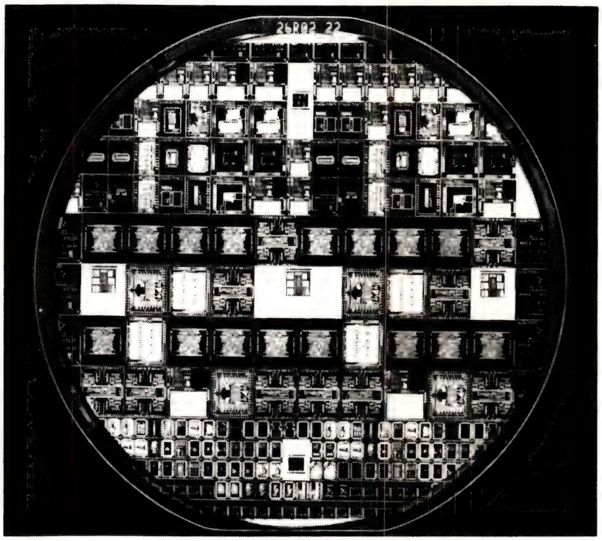

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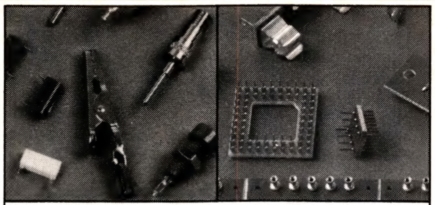

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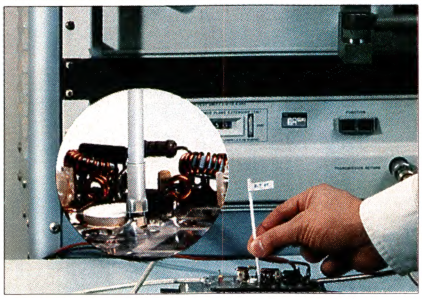

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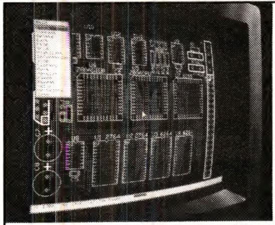

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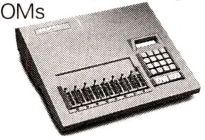

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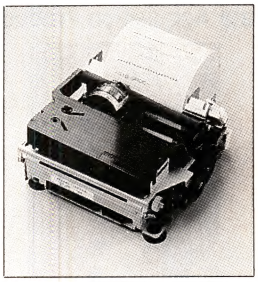

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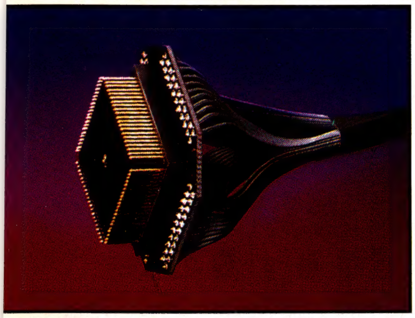

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- Plug your PLCC and LCC packages into your PC board in minutes, with these easy-to-use adapters.
- Emulator/logic analyzer users: Adapt-a-Pod™ converts one package type to another (LCC, PLCC, PGA, and DIPs).
- Emulator pods and adapters are available in all standard pin counts, with ribbon or ribbon cable headers.
- Custom engineering services and do-it-yourself emulator pod converters. Free catalog.

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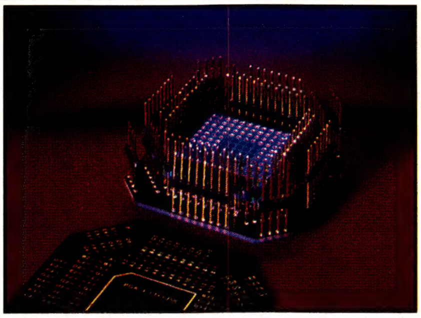
MULATOR PODS & ADAPTERS CIRCLE 526



Complete Line of Debug Tools

- Famous Bug Katcher™ makes it easy to attach test leads to ICs in LCC, PLCC, PGA, PQFP, and DIP packages.
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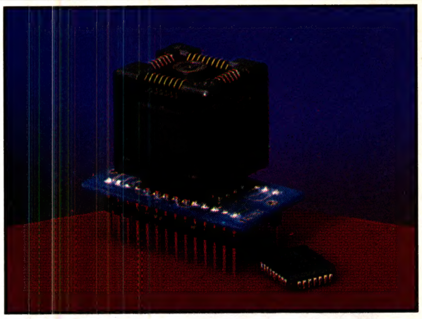

PAL/PROM Programmer Adapters

- Any EPROM programmer designed for DIPs can be converted to accept LCC, PLCC, and SOIC sockets in seconds!
- To program, just insert an Adapt-A-Socket™ between the programmer's DIP socket and the circuit to be programmed.
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- ★ Test Clips (Surfaced Mounted SOIC/PLCC)
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- ★ 125 Types of Programming Socket Converters
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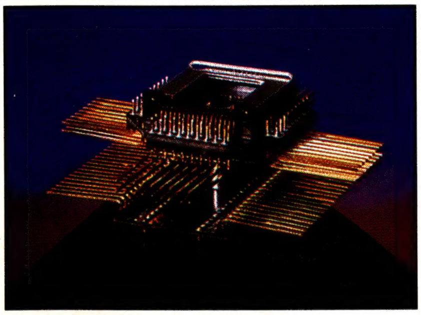
Wrong Prong?

EMULATION TECHNOLOGY CIRCLE 530



Quick, Fast Socket Conversion

- Convert-A-Socket™ makes it a snap to convert a production socket to a test socket and vice-versa.
- Complete line of male/female sockets for LCC, PLCC, PGA, PQFP, and DIP circuits.
- A must if you're inserting circuits repeatedly in low insertion force sockets.
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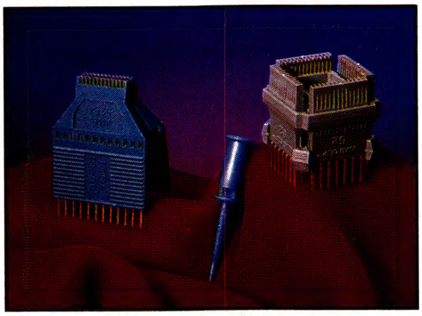

Quality Debugging Accessories

- Protect your ICs from damage. Insert and extract LCC, PLCC, PGA, and PQFP packages with the right tool.
- Use receptacle boards to build test fixtures, and mount your test equipment, in half the time.
- Get the right production sockets, burn-in sockets, test leads, and test clips for SMT, SOIC, or PLCC circuits.
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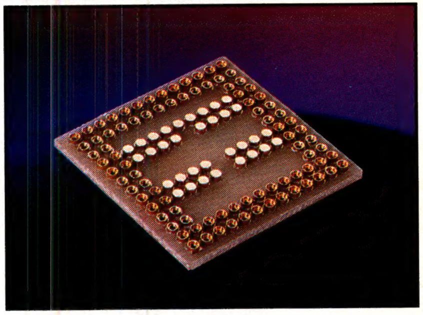

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- For all package types: LCC, PLCC, PGA, PQFP, SDIP (shrink DIP devices), SOIC and more!
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